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Paper 36
Date: June 7, 2021

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG DISPLAY CO., LTD.,
Petitioner,

v.

SOLAS OLED LTD.,
Patent Owner.

IPR2020-00320
Patent 7,446,338 B2

Before SALLY C. MEDLEY, JESSICA C. KAISER, and JULIA HEANEY, *Administrative Patent Judges*.

KAISER, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 318(a)

I. INTRODUCTION

On December 18, 2019, Samsung Display Co. Ltd. ("Petitioner")[1] filed a Petition requesting an *inter partes* review of claims 1–3 and 5–13 of U.S. Patent No. 7,446,338 B2, issued on November 4, 2008 (Ex. 1001, "the '338 patent"). Paper 1 ("Pet."). Solas OLED Ltd. ("Patent Owner") filed a Preliminary Response. Paper 6. Taking into account the arguments presented in Patent Owner's Preliminary Response, we determined the information presented in the Petition established that there was a reasonable likelihood that Petitioner would prevail in challenging at least one of claims 1–3 and 5–13 of the '338 patent, and we instituted this *inter partes* review, as to all challenged claims, on June 23, 2020. Paper 9 ("Dec. on Inst.").

During the course of the trial, Patent Owner filed a Patent Owner Response (Paper 18, "PO Resp."); Petitioner filed a Reply to the Patent Owner Response (Paper 23, "Pet. Reply"); and Patent Owner filed a Sur-reply (Paper 25, "PO Sur-reply"). An oral hearing was held on March 25, 2021, and a transcript of the hearing is included in the record. Paper 35 ("Tr.").

We have jurisdiction under 35 U.S.C. § 6. This decision is a Final Written Decision under 35 U.S.C. § 318(a) as to the patentability of claims 1–3 and 5–13 of the '338 patent. For the reasons discussed below, we hold that Petitioner has demonstrated by a preponderance of the evidence that claims 1–3 and 5–13 are unpatentable.

[1] Apple Inc. filed a petition in IPR2020-01275, and was joined as a petitioner in this proceeding. Paper 24. Subsequently, we granted a joint motion to terminate Apple Inc. as a petitioner in this proceeding, leaving Samsung as the sole remaining petitioner. Paper 31.

II. BACKGROUND

A. The ’338 Patent (Ex. 1001)

The ’338 patent describes a display panel comprised of pixels, the pixels having a particular arrangement of transistors driving the pixels’ light-emitting elements. Ex. 1001, 2:34–41, code (57). Figure 1 of the ’338 patent is reproduced below.

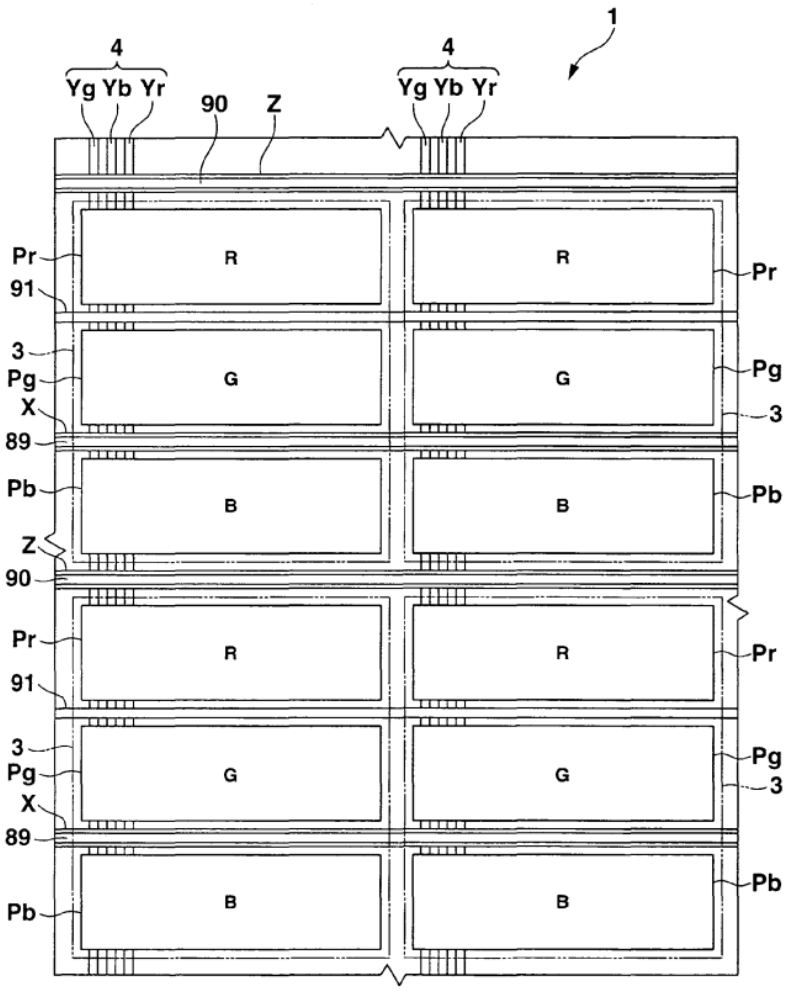


FIG.1

Figure 1 shows four adjacent pixels in display panel 1. Display panel 1 is comprised of pixels 3; in particular, the figure shows four adjacent pixels arranged in a 2-by-2 configuration, i.e., the pixels are arranged in an array.

Id. at 4:53–55, 4:65–66. Each pixel 3 is comprised of red sub-pixel Pr, green sub-pixel Pg, and blue sub-pixel Pb. *Id.* at 4:63–65. Each sub-pixel Pr, Pg, Pb is connected to corresponding signal line Yr, Yb, Yg, respectively. *Id.* at 5:12–15. Further, each sub-pixel is connected to select interconnection 89, feed interconnection 90, and common interconnection 91. *Id.* at 5:23–40; *see id.* at 6:47–48. Still further, each sub-pixel Pr, Pg, Pb have a similar circuit arrangement. *Id.* at 6:47–48.

Figure 2 is reproduced below.

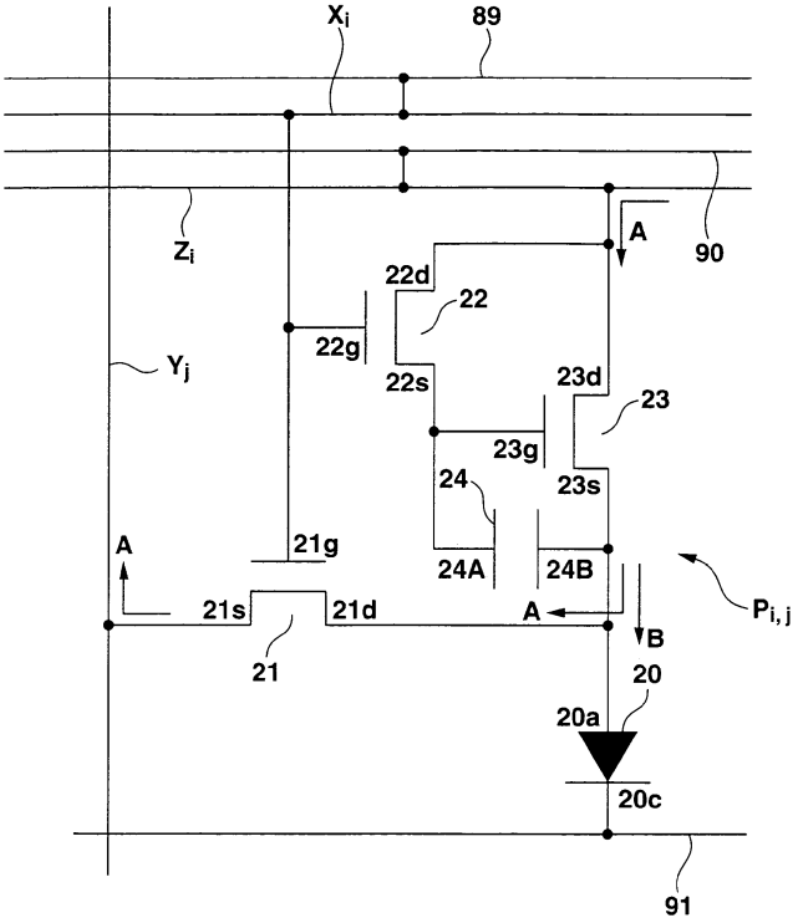


FIG.2

Figure 2 shows the sub-pixel circuit arrangement, which includes organic electroluminescence (EL) element 20, switch transistor 21, holding transistor

22, driving transistor 23, and capacitor 24. *Id.* at 6:48–55. Further, scan line Xi is electrically connected to select interconnection 89, switch transistor 21, and holding transistor 22; signal line Yj is electrically connected to switch transistor 21; and supply line Zi is electrically connected to feed interconnection 90 and driving transistor 23. *Id.* at 6:61–62, 6:65–67, 7:3–6, 7:11–13, 14:47–50.

The '338 patent describes two operating periods for the pixel circuit: a "selection period" and a subsequent "light emission period." *Id.* at 15:28, 15:58–61. During the selection period, a "feed driver applies a write feed voltage VL to supply a write current to the driving transistors 23 connected to" supply line Zi. *Id.* at 14:46–50; *see id.* at Fig. 7. The "write current (pull-out current) . . . flows from the feed interconnection 90 and supply line Zi through the drain-to-source path of the driving transistor 23 and the drain-to-source path of the switch transistor 21" and to signal line Yj. *Id.* at 15:34–41. Notably, "the switch transistor 21 functions to turn on (selection period) and off (light emission period) of the current between the signal line Yj and the source 23s of the driving transistor 23." *Id.* at 17:26–29. That is, switch transistor 21 controls whether the write current flows through driving transistor 23, depending on whether the switch transistor is respectively turned on or off. *See id.*; *see id.* at 15:58–61. In the "subsequent light emission period," switch transistor 21 is "turned off." *Id.* at 15:58–61.

Furthermore, the '338 patent describes that such pixel circuit arrangements for a display are formed "by stacking various kinds of layers on [an] insulating substrate." *Id.* at 8:21–22. Figure 6, reproduced below, is a cross-sectional view of a pixel showing such stacked layers.

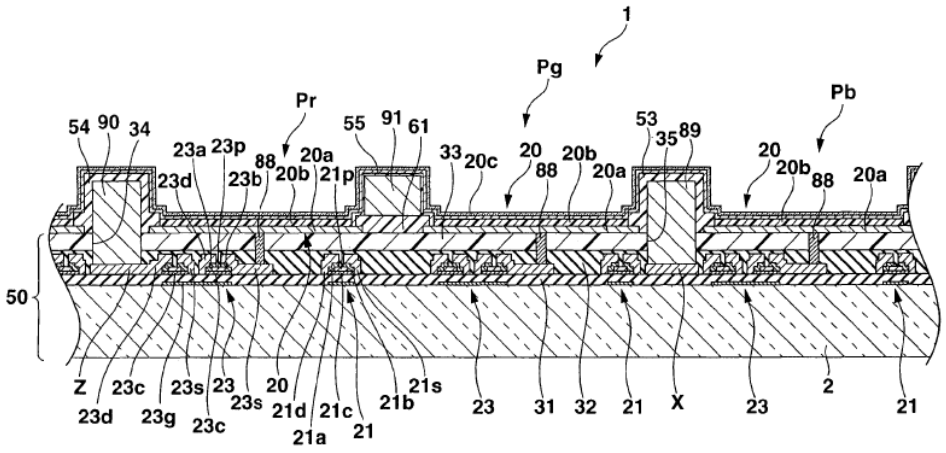


FIG.6

As shown in Figure 6, the aforementioned circuit elements are layered over insulating substrate 2 to form the previously described circuit arrangement. *Id.* at 8:18–53. In particular, transistor array substrate 50 includes transistors 21–23. *Id.* at 8:25–9:2. Interconnections are then stacked to "project upward from the upper surface of the planarization film 33" (*id.* at 11:39–41), i.e., the surface of the transistor array substrate (*id.* at 10:45–47; *see id.* at 10:49–50). Further, "sub-pixel electrodes 20a are arrayed in a matrix on . . . the upper surface of the transistor array substrate 50" (*id.* at 11:50–52) and "organic EL layer 20b of the organic EL element 20," i.e., a light-emitting layer, "is formed on the sub-pixel electrode 20a" (*id.* at 12:14–16). Additionally, "counter electrode 20c functioning as the cathode of the organic EL element 20 is formed on the organic EL layers 20b." *Id.* at 13:28–30.

B. Illustrative claim

Of the challenged claims, claim 1 is independent and is reproduced below.

1. A display panel comprising:

a transistor array substrate which includes a plurality of pixels and comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain;

a plurality of interconnections which are formed to project from a surface of the transistor array substrate, and which are arrayed in parallel to each other;

a plurality of pixel electrodes for the plurality of pixels, respectively, the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate;

a plurality of light-emitting layers formed on the pixel electrodes, respectively; and

a counter electrode which is stacked on the light-emitting layers,

wherein said plurality of transistors for each pixel include a driving transistor, one of the source and the drain of which is connected to the pixel electrode, a switch transistor which makes a write current flow between the drain and the source of the driving transistor, and a holding transistor which holds a voltage between the gate and source of the driving transistor in a light emission period.

Ex. 1001, 24:14–38.

C. Related Proceedings

Petitioner and Patent Owner identify the following related litigation asserting the '338 patent: *Solas OLED Ltd. v. Samsung Display Co., Ltd., et al.*, No. 2:19-cv-00152-JRG (E.D. Tex.);[2] *Solas OLED Ltd. v. Apple Inc.*,

[2] The parties have informed us that there has been a jury verdict in the related Eastern District of Texas proceeding. Ex. 1030, 5:11–6:4, 7:12–17. The jury, however, was not presented with any invalidity arguments as to the '338 patent during that trial. *Id.* Thus, we are presented with different

No. 6:19-cv-00527-ADA (W.D. Tex.); and *Solas OLED Ltd. v. Google Inc.*, No. 6:10-cv-00515-ADA (W.D. Tex.). Pet. 9; Paper 3, 1–2.

D. References

Petitioner relies on the following references:

1. "Kobayashi" (US 2002/0158835 A1; published Oct. 31, 2002) (Ex. 1003);

2. "Shirasaki" (US 2004/0113873 A1; published June 17, 2004) (Ex. 1004); and

3. "Childs" (WO 03/079441 A1; published Sept. 25, 2003) (Ex. 1005).

E. Grounds Asserted

Petitioner asserts that claims 1–3 and 5–13 are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §[3]	References
1, 2, 5, 6, 9–11	103	Kobayashi, Shirasaki
1–3, 5–13	103	Childs, Shirasaki

Petitioner also relies on testimony from Adam Fontecchio, Ph.D. (Ex. 1018). Patent Owner relies on testimony from Richard Flasck (Ex. 2005).

issues to resolve in this Decision than was the jury in the related district court proceeding as to the '338 patent.

[3] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011), amended 35 U.S.C. § 103, effective March 16, 2013. Because the application from which the '338 patent issued was filed before this date, the pre-AIA version of § 103 applies.

III. ANALYSIS

A. Legal Principles

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in the record, objective evidence of nonobviousness.[4] *See Graham v. John Deere Co*., 383 U.S. 1, 17–18 (1966). In that regard, an obviousness analysis "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418.

B. Level of Ordinary Skill in the Art

In the Institution Decision, we adopted Petitioner's formulation of the level of ordinary skill in the art and determined that a person of ordinary skill in the art "would have had a relevant technical degree in electrical engineering, computer engineering, physics, or the like, and 2–3 years of experience in active matrix display design and/or manufacturing." Dec. on Inst. 9 (quoting Pet. 21). In its Patent Owner Response, Patent Owner proposes a similar formulation for the level of ordinary skill in the art. *See* PO Resp. 11–12 (citing Ex. 2005 ¶ 29). We maintain our determination

[4] Neither party presents such evidence in this case.

from the Institution Decision because that level of skill is consistent with the '338 patent and the asserted prior art.

C. Claim Construction

In an *inter partes* review, we construe claim terms according to the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–17 (Fed. Cir. 2005) (en banc). 37 C.F.R. § 42.100(b) (2019). Under that standard, we construe claims "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent." *Id.* Furthermore, we expressly construe the claims only to the extent necessary to resolve the parties' dispute. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Ltd.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

In our Institution Decision, we discussed the terms "write current" and "transistor array substrate" and determined we did not need to explicitly construe those or any other claim terms at that stage of the proceeding. Dec. on Inst. 10–13. We invited the parties to further address the proper constructions of those terms during trial. *Id.* In its trial briefing, Patent Owner addresses claim constructions for the following terms: (1) "transistor array substrate"; (2) "project from a surface of the transistor array substrate"; (3) "write current"; and (4) "the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate." PO Resp. 12–13. Regarding these terms, Patent Owner relies upon the constructions provided in the Claim Construction Memorandum and Order (Ex. 1020) issued in a related district court case

involving these parties and the '338 patent.[5] *Id.* (citing Ex. 1020, 8, 18); *see* Ex. 1020, 8–23. In its Reply, Petitioner addresses constructions for the same terms. Pet. Reply 1–4. For purposes of this decision, we determine we need only address the construction of the following claim terms: (1) "project from a surface of the transistor array substrate," and (2) "the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate." *See Nidec*, 868 F.3d at 1017.

1. "project from a surface of the transistor array substrate"

In the related district court proceeding, the district court construed "project from a surface of the transistor array substrate" to mean "extend beyond an outer surface of the transistor array substrate." Ex. 1020, 15–18.[6] We have considered the district court's claim construction order (37 C.F.R. § 42.100(b)), as well as the parties' arguments, and as discussed in detail below, we adopt the district court's construction of this term as consistent with the ordinary and customary meaning as understood by one of ordinary skill in the art. After considering the parties' arguments in this proceeding, we are not persuaded to adopt any additional refinements to the district court's construction.

Petitioner initially proposed that the term "a plurality of interconnections which are formed to project from a surface of the transistor array substrate" "should be interpreted to encompass a plurality of interconnections which are formed to extend above the upper surface of the

[5] *Solas OLED Ltd. v. Samsung Display Co., Ltd. et al.*, No. 2:19-cv-00152-JRG (E.D. Tex.).

[6] At the district court, the dispute as to this term focused on whether the interconnections must extend beyond an outer surface of the transistor array substrate. Ex. 1020, 15–18; PO Sur-reply 7–8.

topmost layer of the transistor array substrate." Pet. 23–24 (citing Ex. 1018 ¶ 84). Petitioner contends that the disclosure of "the '338 patent defines the 'surface of the transistor array substrate' as the upper surface of the topmost layer of the transistor array substrate, on which pixel electrodes are formed." *Id.* at 23 (citing Ex. 1001, 10:48–51, 11:50–52; Ex. 1018 ¶ 83). Petitioner next addresses "project from" a surface by citing to the embodiment depicted in Figure 6 of the '338 patent and contends that each of the "select interconnection 89, feed interconnection 90, and common interconnection 91 . . . are formed . . . to project [with] respect to the surface of the transistor array substrate 50." *Id.* at 23–24 (quoting Ex. 1001, 12:62–67) (citing Ex. 1001, 10:54–58, 11:36–41, Fig. 6; Ex. 1018 ¶¶ 83–84).

Patent Owner states that it has applied the district court's constructions in its Patent Owner Response. PO Resp. 12. In responding to Petitioner's unpatentability challenges, however, Patent Owner seeks to further limit the district court's construction of "project from a surface of the transistor array substrate." *See id.* at 27, 29–30; PO Sur-reply 3–5. Specifically, Patent Owner argues that this limitation need not be construed to encompass common interconnection 91 in Figure 6 of the '338 patent "[b]ecause the claims at issue use the 'comprising' transition." PO Resp. 28. Relying on the declaration from Mr. Flasck, Patent Owner contends that the district court's "construction . . . requires that there be some connection or relationship between the thing 'projecting' and the surface it is projecting from." *Id.* at 27 (citing Ex. 2005 ¶ 95; Ex. 1020, 17; Ex. 2008, 3 (dictionary definition of "projecting")). Patent Owner further argues that this limitation encompasses structures that "begin near [the transistor array substrate] surface and extend a significant distance away from the surface, both relative to their distance from the surface and relative to their overall

dimensions," but excludes structures that "are far above the surface, relative to their own dimensions, and their extent in the vertical direction (the direction they would need to be 'projecting' or 'protruding'[)] is small relative to the other relevant dimensions." *Id.* at 29–30 (citing Ex. 2005 ¶ 99).

Petitioner replies that the construction proposed in its Petition (Pet. 23–24) "is fully consistent with the district court's construction." Pet. Reply 2–3 (citing Ex. 1020, 18). Petitioner contends that the district court construction of "extend beyond an outer surface of the transistor array substrate" is broader than, but consistent with, Petitioner's proposed construction of "encompass[ing] interconnections which are formed to extend above the upper surface of the topmost layer of the transistor array substrate." *Id.* (citing Pet. 23–24).[7] Petitioner also contends that Patent Owner's attempt to further limit this term is inconsistent with the '338 patent's preferred embodiment describing and depicting common interconnection 91 on top of insulating line 61, which sits on top of the transistor array substrate. *Id.* at 3–4 (citing Ex. 1001, 10:54–58, Fig. 6). Specifically, Petitioner notes that the '338 patent describes common interconnection 91 as "project[ing] upward from the surface of planarization

[7] Petitioner also notes that the district court struck testimony from Patent Owner's district court expert Mr. Credelle that the plain meaning of "project from a surface" and the district court's construction requires "that there be some connection or relationship between the thin[g] 'projecting' and the surface it is projecting from." *See* Pet. Reply 3 (citing PO Resp. 29; Ex. 1026, 88:8–17 (pretrial hearing transcript)); *see also id.* at 15–16 (citing Ex. 1024 ¶ 221; Ex. 1027, 9, 12 (claim construction order)). Patent Owner contends the dispute before the district court was different and thus this argument is a "red herring." PO Sur-reply 7–10.

film 33" (i.e., the transistor array substrate). *See id.* (quoting Ex. 1001, 10:54–58).

In its Sur-reply, Patent Owner emphasizes the importance of "formed to *project from*" and contends "the claim term 'from' introduces an obvious additional spatial requirement beyond just being located above a surface." PO Sur-reply 5. In particular, Patent Owner contends "the [transistor array substrate] surface must [] be a '*starting point*' from which the interconnection projects." *Id.* (citing to dictionary definitions of "from"). Patent Owner cites to the deposition of Petitioner's expert, Dr. Fontecchio, and asserts that Dr. Fontecchio and Petitioner misinterpret "project from a surface" as "formed anywhere above a surface." *Id.* at 4 (citing Ex. 2007, 121:9–11) (emphasis omitted).

After having reviewed the claim language, the arguments, and the evidence, we determine that the district court's construction of "project from a surface of the transistor array substrate" is consistent with the ordinary and customary meaning of the phrase in light of the Specification, and we adopt that construction for purposes of this Decision. We have considered the additional requirements as asserted by Patent Owner, but do not find them supported by the evidence as discussed below.

Turning first to the claim language, we agree with Patent Owner that the plain meaning of the term, and the district court's construction, requires "some connection or relationship between the thing 'projecting' and the surface it is projecting from." PO Resp. 27 (citing Ex. 1020, 17; Ex. 2005 ¶ 95; Ex. 2008, 3). The district court relied on a dictionary definition of "project" to inform that relationship as "extend[ing] outward beyond something else," i.e., extending outward beyond the transistor array substrate. Ex. 1020, 17–18. Here, Patent Owner goes further and relies

upon dictionary definitions[8] of "from" to further limit the surface of the transistor array substrate as the "starting point" from which the interconnection projects. PO Sur-reply 5. We do not interpret these definitions to narrowly limit "from" in the way Patent Owner argues. In the disputed limitation, the surface of the transistor array substrate is a point of reference and the interconnection extends in a direction away from the surface; thus there is a relationship between the thing projecting (i.e., the interconnection) and the surface it is projecting from (that of the transistor array substrate). While we agree with Patent Owner that "[e]ach element contained in a patent claim is deemed material to defining the scope of the patent invention" (*id.* (citing *Warner-Jenkinson Co. v. Hilton Davis Chem. Co.*, 520 U.S. 17 (1997)), the district court's construction as "extend beyond" does not read any sort of positional or spatial requirements out of the claim limitation.

Turning to the Specification, the '338 patent discloses that "[t]he common interconnection 91 is formed by electroplating and is therefore formed to . . . project upward from the surface of the planarization film 33" (i.e., "the upper surface of the transistor array substrate 50"). Ex. 1001, 10:52–58, 11:50–52. In addition, the '338 patent also describes "select interconnection 89, feed interconnection 90, and common interconnection 91 . . . are formed between the sub-pixel electrodes 20a adjacent in the vertical direction to project [with] respect to the surface of the transistor array

[8] Because a sur-reply may not be accompanied by new evidence (37 C.F.R. § 42.23(b)), Patent Owner provides only websites for these definitions. Although it is generally improper to introduce evidence in this way in a sur-reply, we have considered these definitions in this instance because they inform our understanding of Patent Owner's claim construction arguments, which we find unpersuasive for the reasons explained below.

substrate 50." *Id.* at 12:62–67. Although Patent Owner is correct that the transitional phrase "comprising" in claim 1 is non-limiting (PO Resp. 28), the written description of the '338 patent describes common interconnection 91 as being formed to project from the surface of the transistor array substrate. In other words, even though common interconnection 91 does not have planarization film 33 as its starting point (*see* Ex. 1001, Fig. 6 (depicting insulating line 61 between common interconnection 91 and planarization film 33)), the written description describes common interconnection 91 as projecting upward from the surface of planarization film 33 (*id.* at 10:54–58). Thus, the written description makes clear that "project from" does not exclude such intermediate structures.

We are also not persuaded that the '338 patent Specification requires any specific relative dimensions for the interconnection to "project from" the surface of the transistor array substrate. The '338 patent discloses "[t]he common interconnection 91 is formed by electroplating and is therefore formed to be much thicker than the signal line Y, scan line X, and supply line Z and project upward from the surface of the planarization film 33 [i.e., the surface of the transistor array substrate]." *Id.* at 10:54–58. The '338 patent also discloses "[t]he thick select interconnection 89, feed interconnection 90, and common interconnection 91 whose tops are much higher than that of the insulating line 61 are formed between the sub-pixel electrodes 20a adjacent in the vertical direction to project [with] respect to the surface of the transistor array substrate 50." *Id.* at 12:62–67. Regarding interconnections 89 and 90, the '338 patent discloses:

> The select interconnections 89 and feed interconnections 90 are formed by electroplating and are therefore much thicker than the signal lines Y, scan lines X, and supply lines Z. The thickness of the select interconnection 89 and feed interconnection 90 is

> larger than the total thickness of the protective insulating film 32 and planarization film 33 so that the select interconnection 89 and feed interconnection 90 project upward from the upper surface of the planarization film 33 [i.e., surface of the transistor array substrate].

Id. at 11:33–41.

We view these disclosures as non-limiting descriptions of a preferred embodiment of the '338 patent. *See id.* at 4:46–48 ("[T]he spirit and scope of the present invention are not limited to the following embodiments and illustrated examples."). We observe that in the Figure 6 embodiment, select interconnection 89 and feed interconnection 90 begin below planarization film 33 within protective film 32, and thus the Specification describes those interconnections as being larger than the total thickness of both films so that those interconnections project from (i.e., "extend beyond") the outer surface of the transistor array substrate. In contrast, the Specification states that "common interconnection 91 is formed by electroplating and is therefore formed to be much thicker than the signal line Y, scan line X, and supply line Z and project upward from the surface of the planarization film 33." Ex. 1001, 10:54–58. In other words, the Specification identifies a relative thickness for the common interconnection in the Figure 6 embodiment as compared to the signal line Y, scan line X, and supply line Z, but does not indicate that that relative thickness is required for common interconnection 91 to project from the surface of planarization film 33. We also agree with Petitioner that "[n]othing in the '338 patent's claims or specification indicates the term 'project from' has any relationship to the thickness of the insulating layer between an interconnection and the transistor array substrate." Pet. Reply 18–19 (citing PO Resp. 29–30). Thus, we find that the Specification of the '338 patent does not require the further limitations

that Patent Owner argues we should adopt in the construction of "project from a surface of the transistor array substrate."[9]

For the foregoing reasons, we agree with the district court's construction of "project from a surface of the transistor array substrate" as "extend beyond an outer surface of the transistor array substrate" (Ex. 1020, 15–18), and we do not adopt Patent Owner's proposed further limitations to this construction.

2. "the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate"

The district court construed "the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate" to mean "the pixel electrodes are arrayed along the interconnections and located between the interconnections, and the pixel electrodes are on the surface of the transistor array substrate." Ex. 1020, 8 & n.2. As Petitioner indicates, "[t]he district court adopted this as an agreed construction." Pet. Reply 2 (citing Ex. 1020, 8); *see also* Ex. 1020, 8 n.2 ("[T]he Court finds that the parties' agreed construction of this term comports with [the] Court's view."). We have considered the district court's claim construction order (37 C.F.R. § 42.100(b)), as well as the parties' arguments, and as discussed in detail below, we adopt the district court's claim construction of this term as consistent with the ordinary and customary meaning as understood by one of ordinary skill in the art. After considering

[9] Although the prosecution history of the '338 patent is in the record (Ex. 1002) and discussed as background in the Petition (Pet. 19–21) and Patent Owner Response (PO Resp. 9–11), we note that neither Petitioner nor Patent Owner specifically argues that the prosecution history affects the proper construction of this claim term.

the parties' arguments in this proceeding, we are not persuaded to adopt any additional refinements to the district court's construction.

Petitioner initially proposed that "the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate" means "that the pixel electrodes: (1) are arrayed along the interconnections between the interconnections; and (2) are arrayed on the surface of the transistor array substrate." Pet. 25 (citing Ex. 1018 ¶ 85). Petitioner supports this construction by citing to the disclosure of the '338 patent that states "[t]he plurality of sub-pixel electrodes 20a are arrayed in a matrix on the upper surface of the planarization film 33, i.e., the upper surface of the transistor array substrate," and "these sub-pixel electrodes are arrayed between the interconnections 89, 90, and 91 . . . as depicted in [] Figure 6." *Id.* (citing Ex. 1001, 11:50–52, 12:30–54, Fig. 6; Ex. 1018 ¶ 86).

Patent Owner states that it has applied the district court's constructions in its Patent Owner Response. PO Resp. 12. In responding to Petitioner's unpatentability challenges, however, Patent Owner seeks to further limit the district court's construction of "the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate." *See id.* at 32, 44–45; PO Sur-reply 13–19, 22–23, 25–26. Relying on the declaration from Mr. Flasck, Patent Owner contends that if "[parts] or portions of the pixel electrodes are *almost directly below* [*or beneath*] the interconnections," then those pixel electrodes "are not 'arrayed along' or 'located between' the interconnections, as those terms would be understood by" a person of ordinary skill in the art. PO Resp. 32, 45 (citing Ex. 2005 ¶¶ 104, 133) (emphasis added). Patent Owner further contends that if "large portions of the pixel electrodes are buried

within and under the transistor array substrate," then those electrodes are not "on the surface" of the transistor. *Id.* at 44 (citing Ex. 2005 ¶ 133).

Petitioner replies that the construction proposed in its Petition is consistent with the agreed upon construction of "the pixel electrodes are arrayed along the interconnections and located between the interconnections, and the pixel electrodes are on the surface of the transistor array substrate." Pet. Reply 2 (citing Ex. 2004, 1; Ex. 1020, 8). Petitioner argues that being "arrayed along and between" does not require the electrodes and the interconnections to be "coplanar." *Id.* at 20–21, 28 (citing PO Resp. 44–45). In support, Petitioner relies on Figure 6 of the '338 patent and its associated description. *Id.* at 20–21 (citing Ex. 1001, 5:61–66, Fig. 6). Petitioner next argues that being "arrayed . . . on the surface" of the transistor array substrate does not preclude an overlap of the transistor array substrate on a portion of the electrodes. *Id.* at 29.

In its Sur-reply, Patent Owner contends that because the pixel electrodes and the interconnections of the asserted art are not coplanar and "***do not share any overlapping layers***," then such structures cannot be "arrayed along." PO Sur-reply 13–14, 17. Relying on dictionary definitions, Patent Owner asserts that a person of ordinary skill in the art "would understand this plain requirement of being arrayed 'along' to demand a showing that the electrode is arrayed '*in a[] line matching the length or direction of*' the interconnections." *Id.* at 15 (citing dictionary definitions of "along").[10] Patent Owner also contends the disclosure of the

[10] As with the "project from" limitation, because a sur-reply may not be accompanied by new evidence (37 C.F.R. § 42.23(b)), Patent Owner provides only websites for these definitions. Although it is generally improper to introduce evidence in this way in a sur-reply, we have

’338 patent “demands this as well” and cites to portions of the ’338 patent that “describe[] the process of elements of the preferred embodiments being formed or arrayed *alongside* others.” *Id.* (citing Ex. 1001, 2:45–47, 5:61–6:2, 7:44–8:15, 10:48–11:65, 12:30–13:17, Figs. 1, 3–6).

Patent Owner further contends that even if the “arrayed along” limitation does not require the pixel electrodes and interconnections to be in the “same plane or layer,” the limitation “must imply being adjacent to one another and some overlap in at least one of the interconnections.” *Id.* at 17, 25. Patent Owner contends Petitioner’s “coplanar” argument misunderstands Patent Owner’s plain meaning interpretation and builds a strawman. *Id.* at 19 (citing Pet. Reply 20–21). Patent Owner further contends that Petitioner’s reliance on a single sentence from the disclosure of the ’338 patent to support its position is misplaced because the sentence relied upon “is directed to a single embodiment [that is depicted in Figure 2 and not Figure 6] and [] *does not even mention the phrase ‘arrayed along.*’” *Id.* at 20 (citing Pet. Reply 21). Patent Owner also contends that even if reliance upon the embodiment depicted in Figure 6 is proper, that embodiment “does not support [Petitioner’s] argument[, because] it shows the [] pixel electrodes sharing overlapping horizontal portions with a plurality of interconnections 90 and 89 and even shows [pixel electrodes] ***adjacent*** to the third interconnection 91.” *Id.*

For the “on the surface” requirement of this limitation, Patent Owner contends that if “large portions of the pixel electrodes are buried ***under and***

considered these definitions in this instance because they inform our understanding of Patent Owner’s claim construction arguments, which we find unpersuasive for the reasons explained below.

in the alleged substrate," then such electrodes are not "on the surface" of the transistor array substrate. *Id.* at 22 (citing Ex. 2005 ¶ 133).

After having reviewed the claims, the arguments, and the evidence, we determine that the district court's construction of this term to mean "the pixel electrodes are arrayed along the interconnections and located between the interconnections, and the pixel electrodes are on the surface of the transistor array substrate" is consistent with the ordinary and customary meaning of the phrase in light of the Specification, and we adopt that construction here. Furthermore, we have considered the additional requirements as asserted by Patent Owner, but do not find them supported by the evidence as discussed below.

Turning first to the claim language, we do not agree with Patent Owner that the plain language of "the pixel electrodes being arrayed along the interconnections" or "the pixel electrodes being arrayed . . . between the interconnections" precludes an arrangement of the electrodes with respect to the interconnections such that one is almost directly below or beneath the other. PO Resp. 32, 45 (citing Ex. 2005 ¶¶ 104, 133). We also do not agree with Patent Owner that "being arrayed along" further requires either (1) sharing of overlapping layers or (2) being adjacent and also sharing some overlap in at least one of the interconnections. PO Sur-reply 13–17 (citing Ex. 2005 ¶ 104). Patent Owner cites to nothing in the claim language to support its assertion that "along" requires some degree of overlapping layers, but seems to base this argument on the asserted reference's configuration in addressing Petitioner's unpatentability grounds. *See id.* at 14–16. Patent Owner also provides no support for its arguments that even if "arrayed along" does not require the pixel electrodes and the interconnection to be in the same plane or layer, such a "requirement must imply being adjacent to

one another and some overlap in at least one of the interconnections." *Id.* at 17. Patent Owner does, however, provide support for the understanding "of being arrayed 'along' to demand a showing that the electrode is arrayed '*in a[] line matching the length or direction of*' the interconnections." *Id.* at 15 (citing dictionary definitions of "along"). These definitions, however, do not preclude an arrangement of the electrodes with respect to the interconnections such that one is almost directly below or beneath the other. In other words, these structures can still be in the same direction even if one sits below the other in a cross-sectional view.

Regarding the claim language of "the pixel electrodes being arrayed . . . on the surface of the transistor array substrate," we do not agree with Patent Owner that being arrayed on the surface precludes edge portions of the pixel electrodes from being buried under the transistor array substrate. PO Resp. 44 (citing Ex. 2005 ¶ 133); PO Sur-reply 22–23 (citing Ex. 2005 ¶ 133). We do not find the plain language of this limitation to require that the entirety of the pixel electrodes be arrayed on the surface of the transistor array substrate.

Turning to the Specification of the '338 patent, we find helpful the portions of the disclosure Patent Owner cites as describing the "arrayed along" limitation. PO Sur-reply 15 (citing Ex. 1001, 2:45–47, 5:61–6:2, 7:44–8:15, 10:48–11:65, 12:30–13:17, Figs. 1, 3–6). In particular, Figure 1 depicts a plurality of sub-pixel electrodes 20a arrayed in a matrix, with each pixel represented by a rectangle long in the horizontal direction, i.e., the left-to-right direction of Figure 1. Ex. 1001, 5:51–60, Figs. 1–2. The sub-pixel electrodes 20a are further described as being "arrayed in the horizontal direction" between various interconnections, for example, "between the feed interconnection 90 and the adjacent common interconnection 91." *Id.* at

5:61–6:2. Thus, in terms of "arrayed along," the sub-pixel electrodes in this embodiment extend in a direction or line matching the direction of the interconnections.[11]

The disclosure of the '338 patent further describes the planar layout of the pixels as depicted in Figures 3–5. *Id.* at 7:52–8:15, Figs. 3–5. This disclosure provides that various structures are "arranged along" other structures, most notably the switch transistor 21 and driving transistor 23 being arranged along common interconnection 91. *Id.* While the description of structures being "arranged along" other structures is in reference to Figures 3–5, Figure 6 depicts a sectional view taken along a line in Figures 3–5 and best illustrates whether being "arranged along" precludes being located almost directly below or beneath or requires being "adjacent to one another and some overlap in at least one of the interconnections." With reference to the description as noted above, Figure 6 depicts both switch transistor 21 and driving transistor 23 as not overlapping with any layer shared by common interconnection 91. *Id.* at 7:54–55, 7:59–60, Fig. 6. In addition, driving transistor 23 is described as being arranged along both supply line Z and feed interconnection 90, but driving transistor 23 again does not overlap with any layer shared by supply line Z or feed interconnection 90. *Id.* at 7:53–54, Fig. 6. Although "arranged along" is different terminology than "arrayed along," both use "along," and we find

[11] We do not view this disclosure as limited to only Figure 2, as Patent Owner appears to argue. *See* PO Sur-reply 20 (citing Pet. Reply 21). The cited portion of the '338 patent refers to the planar layout of display panel 1. *See* Ex. 1001, 4:51. Figure 6 depicts the layer structure (i.e., a cross-sectional view) of display panel 1. *See id.* at 8:17–20. We do not understand the written description of the '338 patent as disclosing these figures as separate embodiments to be viewed in isolation.

that the "arranged along" descriptions support that a person of ordinary skill in the art would not understand "arrayed along" to require some overlap in at least one of the interconnections as asserted by Patent Owner.

The Specification of the '338 patent further describes the "between" relationship for interconnections and sub-pixel electrodes. *Id.* at 5:31–38, 5:53–57. In particular, the '338 patent describes common interconnection 91 as being arranged between the red and green sub-pixels Pr and Pg, denoted 20a in Figure 6. *Id.* at 5:31–33, 5:53–57, Fig. 6. The '338 patent also describes scan line X and select interconnection 89 as being arranged between green and blue sub-pixels Pg and Pb, and supply line Z and feed interconnection 90 as being arranged between blue and red sub-pixels Pb and Pr. *Id.* at 5:33–38, 5:53–57, Fig. 6. Thus, the "between" arrangement as described and depicted by the '338 patent does not require a degree of overlap in the vertical direction (as viewed from the side-sectional view of Figure 6); instead, this description allows for structures arrayed between other structures regardless of how they are disposed in cross-section (e.g., pixel electrodes being almost directly below common interconnection 91 as depicted in Figure 6).

Turning to the '338 patent's description of "on the surface," the Specification describes several structures as being "on the surface" of others. For example, insulating line 61 is "formed on the surface of the planarization film 33, i.e., on the surface of the transistor array substrate 50," and "[t]he plurality of sub-pixel electrodes 20a are arrayed in a matrix on the upper surface of the planarization film 33, i.e., the upper surface of the transistor array substrate." *Id.* at 10:48–50, 11:50–52. Other structures, however, are described differently. Common interconnection 91 is formed to "project upward from the surface of the planarization film 33," and similarly, select

interconnection 89 and feed interconnection 90 "project upward from the upper surface of the planarization film 33." *Id.* at 10:54–58, 11:36–41. As depicted in Figure 6, structures such as insulating line 61 and sub-pixel electrodes 20a are disposed directly on the surface of the planarization film 33 whereas interconnections 89, 90, and 91 are either disposed slightly above or below the upper surface of the planarization film 33, and thus, are not on the surface. Therefore, the '338 patent describes "on the surface" as being disposed directly on the surface, but does not restrict "on the surface" to require that the entirety of the structure be disposed directly on the surface.

For the foregoing reasons, we determine that the limitation "the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate" means "the pixel electrodes are arrayed along the interconnections and located between the interconnections, and the pixel electrodes are on the surface of the transistor array substrate" as construed by the district court. Ex. 1020, 8 & n.2. As discussed above, we do not adopt Patent Owner's proposed further limitations to this construction.

D. Asserted Obviousness over Kobayashi and Shirasaki

1. Overview of Kobayashi (Ex. 1003)

Kobayashi describes "a planar display device such as an organic electroluminescence (EL) display device" which "includes display elements arranged in a matrix and auxiliary wiring elements." Ex. 1003 ¶ 1, code (57). The arrangement of display elements and auxiliary wiring elements is shown below in Figure 1.

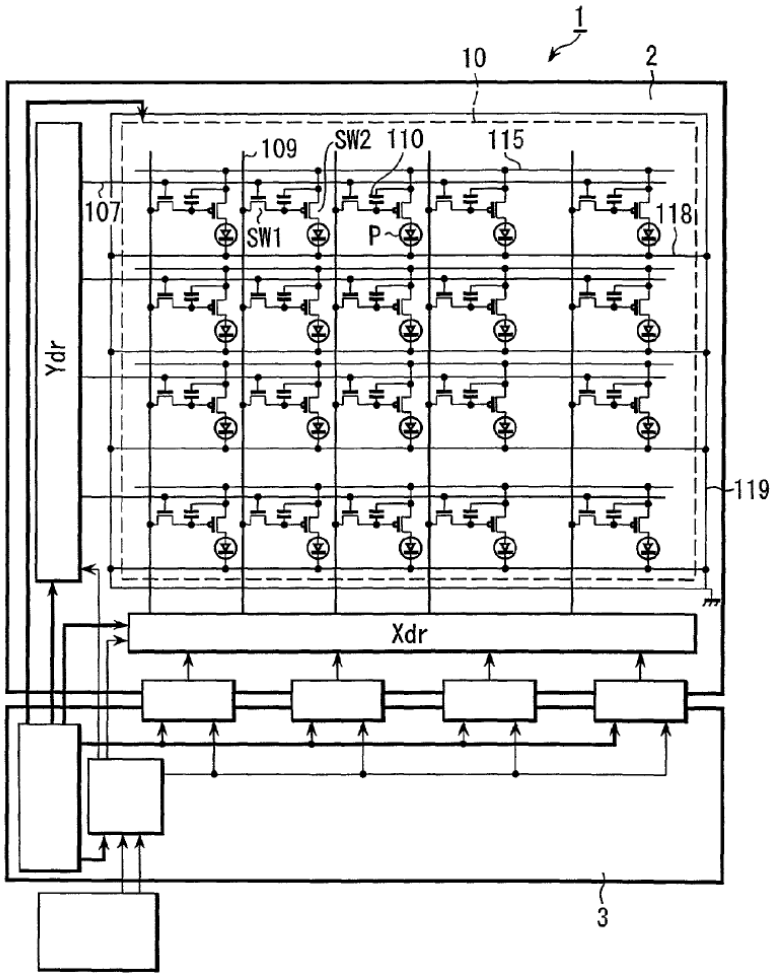
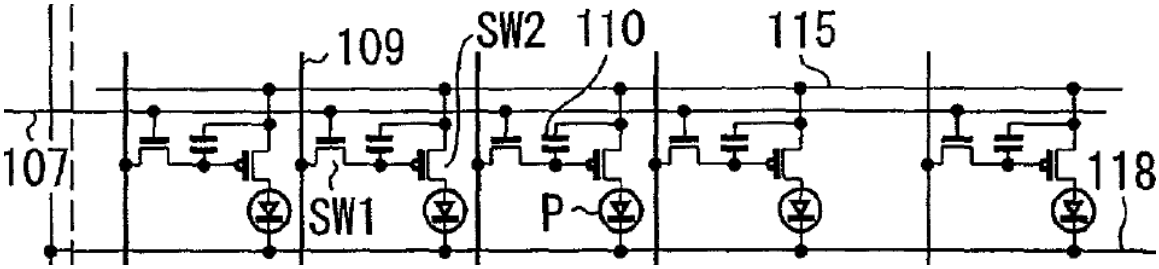


FIG. 1

As shown in Figure 1, organic EL display device 1 has "a display region 10 where the display elements P are arranged in a matrix." *Id.* ¶ 41. There are "three kinds of display elements P, which respectively emit red, green and blue light." *Id.* Further, the display "includes an n-type TFT functioning as a switching element SW1, a capacitor 110 for holding a video signal voltage, [and] a p-type TFT functioning as a driving control element SW2." *Id.* ¶ 43. The display still further includes signal lines, in particular, "scan signal line drive circuit Ydr for supplying drive pulses to the scan

signal lines 107 and a video signal line drive circuit Xdr for supplying drive signals to the video signal lines 109." *Id.* ¶ 42.

The arrangement of the display components is shown below, in an enlarged portion of Figure 1.



As shown in the enlarged portion of Figure 1, "driving control element SW2 is connected in series to the organic EL display element P." *Id.* ¶ 43. In particular, driving control element SW2 connects organic EL display element P to "an organic EL current supply line 115." *See id.* ¶ 70. Further, "video signal voltage holding capacitor 110 is connected in series to the switching element SW1 and in parallel to the driving control element SW2." *Id.* ¶ 43.

Furthermore, Kobayashi's display elements and associated interconnections may be formed in layers on an insulating support substrate, as shown below in Figure 7.

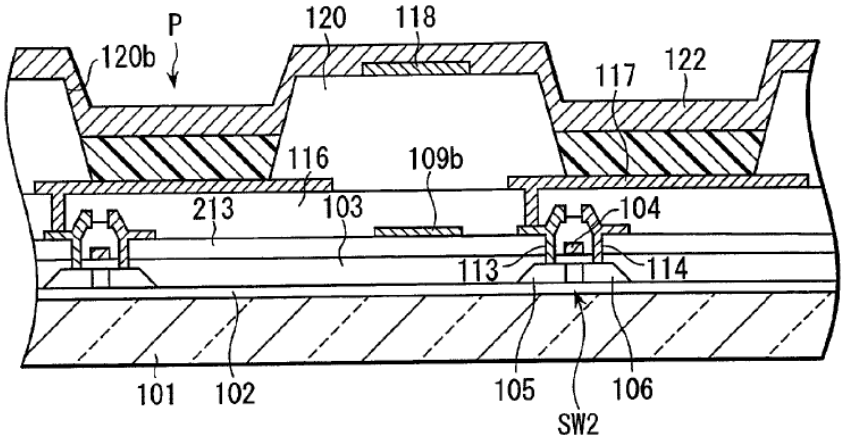


FIG. 7

Figure 7 shows a partial cross-sectional view of the structure of the display region of Kobayashi's organic EL display device. *Id.* ¶ 35. In particular, Figure 7 shows:

> first electrode 117 formed of a light-reflecting conductive film, which is connected to the driving control element SW2; an organic light-emission layer 121 functioning as a light active layer, which is disposed on the first electrode 117; and a second electrode 122 disposed to be opposed to the first electrode 117 via the organic light-emission layer 121.

Id. ¶ 44. Figure 7 also shows:

> auxiliary wiring elements 118 electrically connected to the second electrode 122 are disposed in a lattice shape on partition walls 120 that electrically isolate the pixels in the display region 10. Each auxiliary wiring element 118 is commonly electrically connected to the second electrode power supply line 119 for supplying power to the second electrode 122. The auxiliary wiring elements 118 are interconnected over the entire display region 10.

Id. ¶ 88.

2. Overview of Shirasaki (Ex. 1004)

Shirasaki describes a "circuit configuration of [a] pixel driving circuit" for a display panel. Ex. 1004 ¶¶ 1, 68. Figure 5B of Shirasaki is reproduced below.

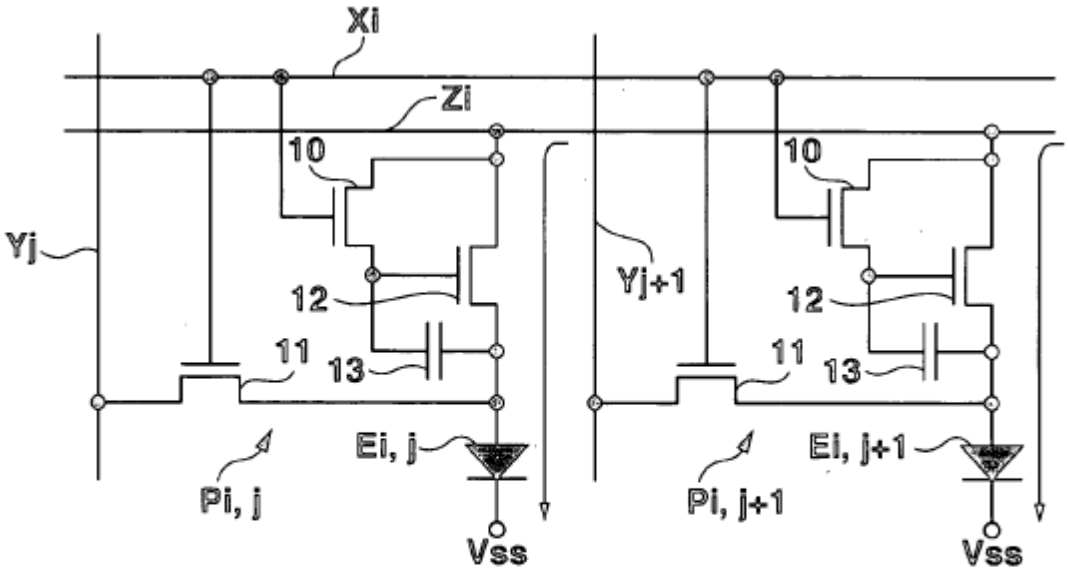


FIG.5B

Figure 5B shows a circuit diagram for driving two adjacent pixels during a non-selection period. *Id.* ¶¶ 32, 44. The pixel driving circuit for pixel Pi, j (the pixel on the left-hand side of Figure 5B) includes three transistors 10, 11, and 12, capacitor 13, and organic EL element Ei, j. *Id.* ¶ 68. During a selection period, transistor 11 is turned on, and a current is supplied "between the source and drain of the transistor 12 through the current line Y_j in accordance with the image data." *Id.* ¶¶ 84, 92. Also during the selection period, "transistor 10 is turned on . . . and a voltage is applied to . . . capacitor 13" (*id.* ¶ 84) which "stores electric charge, as current data, which has a magnitude corresponding to the current value" (*id.* ¶¶ 72, 91). During a non-selection period, transistor 11 is turned off and "display current equal to the extracted memory current [is supplied] to the organic EL element E." *Id.* ¶¶ 88, 92. In particular, "transistor 12 can supply a desired electric current corresponding to the image data" to organic EL element Ei, j. *Id.* ¶ 92.

3. Analysis

Petitioner contends that claims 1, 2, 5, 6, and 9–11 are unpatentable as obvious over Kobayashi and Shirasaki. Pet. 38–62; Pet. Reply 4–21. We have reviewed the evidence and arguments provided by the parties and are persuaded that Petitioner has demonstrated by a preponderance of the evidence that claims 1, 2, 5, 6, and 9–11 are unpatentable as obvious over Kobayashi and Shirasaki.

Claim 1

Claim 1 recites "[a] display panel." Ex. 1001, 24:14. Petitioner contends that Kobayashi teaches this limitation. Pet. 39. In particular, Petitioner contends Kobayashi discloses "an active matrix type planar display device." *Id.* (citing Ex. 1003 ¶ 1; Ex. 1018 ¶ 103).

We determine Petitioner has shown Kobayashi teaches this limitation of claim 1. Kobayashi discloses that "[t]he present invention relates to a planar display device such as an organic electroluminescense (EL) display device." Ex. 1003 ¶ 1. We find this disclosure, cited by Petitioner, shows that Kobayashi discloses "[a] display panel" as recited in claim 1. We note that Patent Owner does not separately address this limitation (*see generally* PO Resp.; PO Sur-reply).

Claim 1 further recites "a transistor array substrate which includes a plurality of pixels and comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain." Ex. 1001, 24:15–18. Petitioner contends Kobayashi teaches this limitation. Pet. 39–43. In particular, Petitioner argues Kobayashi's layered structure as depicted in Figure 7 teaches the "transistor array substrate," which extends from "insulating support substrate 101" to "insulating layer 116," and that a person of ordinary skill in the art would have understood

Kobayashi's layered structure as such. *Id.* at 39–40 (citing Ex. 1003 ¶¶ 64, 73, 80, Fig. 7; Ex. 1018 ¶ 106–107). Petitioner further contends Kobayashi's layered structure teaches an "organic EL panel 2" that contains multiple "display elements P" – pixels. *Id.* at 40–42 (citing Ex. 1003 ¶¶ 41, 90–91; Ex. 1018 ¶¶ 109–110). Petitioner also contends for each of Kobayashi's display elements, "the organic EL panel 2 includes an n-type TFT [transistor] functioning as a switching element SW1" and "a p-type TFT [transistor] functioning as a driving control element SW2" and that each thin film transistor SW1 and SW2 includes, respectively, a gate electrode 104, 108, a gate insulating film 103, a source region 105, 111 connected to a source electrode 113, 132, and a drain region 106, 112 connected to a drain electrode 114, 131. *Id.* at 42–43 (citing Ex. 1003 ¶¶ 43, 66, 68–71, Fig. 7; Ex. 1018 ¶¶ 111–114).

We determine Petitioner has shown Kobayashi teaches this limitation of claim 1. Kobayashi depicts a layered structure in Figure 7 and describes the layered structure as including insulating support substrate 101, an undercoat layer 102 formed thereon, and an insulating layer 116 with pixel electrodes 117 formed on the insulating layer 116. Ex. 1003 ¶¶ 64, 73–74, 80. Kobayashi further discloses a plurality of display elements P as pixels arranged in a matrix in display region 10. *Id.* ¶ 41. Kobayashi also discloses the organic EL panel 2 includes n-type and p–type thin film transistors (TFTs) SW1, SW2 and that electrode 117 is formed on the TFTs via insulating layer 116. *Id.* ¶¶ 43, 60, 84. Kobayashi further discloses that each TFT SW1, SW2 includes a source region connected to a source electrode, a drain region connected to a drain electrode, a gate insulating film, and a gate. *Id.* ¶¶ 66, 68–71. We find these disclosures, cited by Petitioner, show that Kobayashi discloses "a transistor array substrate which

includes a plurality of pixels and comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain" as recited in claim 1. We note that Patent Owner does not separately address this limitation (*see generally* PO Resp.; PO Sur-reply).

Claim 1 further recites "a plurality of interconnections which are formed to project from a surface of the transistor array substrate, and which are arrayed in parallel to each other." Ex. 1001, 24:19–21. For this limitation, Petitioner contends "Kobayashi discloses 'auxiliary wiring elements 118 [that] are interconnected over the entire display region 10' and that project from the surface of 'insulating layer 116' (i.e., the surface of the claimed transistor array substrate)." Pet. 44–45 (citing Ex. 1003 ¶¶ 88, Fig. 7; Ex. 1018 ¶ 115). Petitioner further contends that much like the purpose of the common interconnection 91 in the '338 patent is to "reduce the sheet resistance of the cathode electrode," Kobayashi discloses the "'auxiliary wiring elements 118' are 'electrically connected to the second electrode 122' [and] lower[] the resistance of that electrode 122 to improve the uniform appearance of the display screen." *Id.* (citing Ex. 1001, 14:8–19; Ex. 1003 ¶¶ 62, 83; Ex. 1018 ¶ 116). Petitioner contends Figure 7 of Kobayashi depicts the "'auxiliary wiring element 118' [being] formed on 'partition walls 120' and extend[ing] above the surface of insulating layer 116," which Petitioner further contends is like Figure 6 of the '338 patent depicting "common interconnections 91 [being] formed on 'insulating line 61' and extend[ing] above the surface of transistor array substrate 50." *Id.* at 45 (citing Ex. 1001, Fig. 6; Ex. 1003 ¶ 88, Fig. 7; Ex. 1018 ¶ 117). Petitioner further contends Kobayashi's "'auxiliary wiring elements 118' (the claimed plurality of interconnections) are arrayed in parallel to each other: 'auxiliary

wiring elements 118 . . . are disposed in a lattice shape.'" *Id.* at 45–46 (quoting Ex. 1003 ¶ 88; citing *id.* at Fig 1; Ex. 1018 ¶ 118).

In its Patent Owner Response, Patent Owner largely focuses on its claim construction arguments discussed above in arguing that Kobayashi does not teach this limitation of claim 1. *See* PO Resp. 26–30. Specifically, Patent Owner argues that auxiliary wiring elements 118 of Kobayashi do not "project from a surface" because "[t]hey are far above the surface, relative to their own dimensions, and their extent in the vertical direction (the direction they would need to be 'projecting' or 'protruding'[)] is small relative to the other relevant dimensions." *Id.* at 29–30 (citing Ex. 2005 ¶ 99).

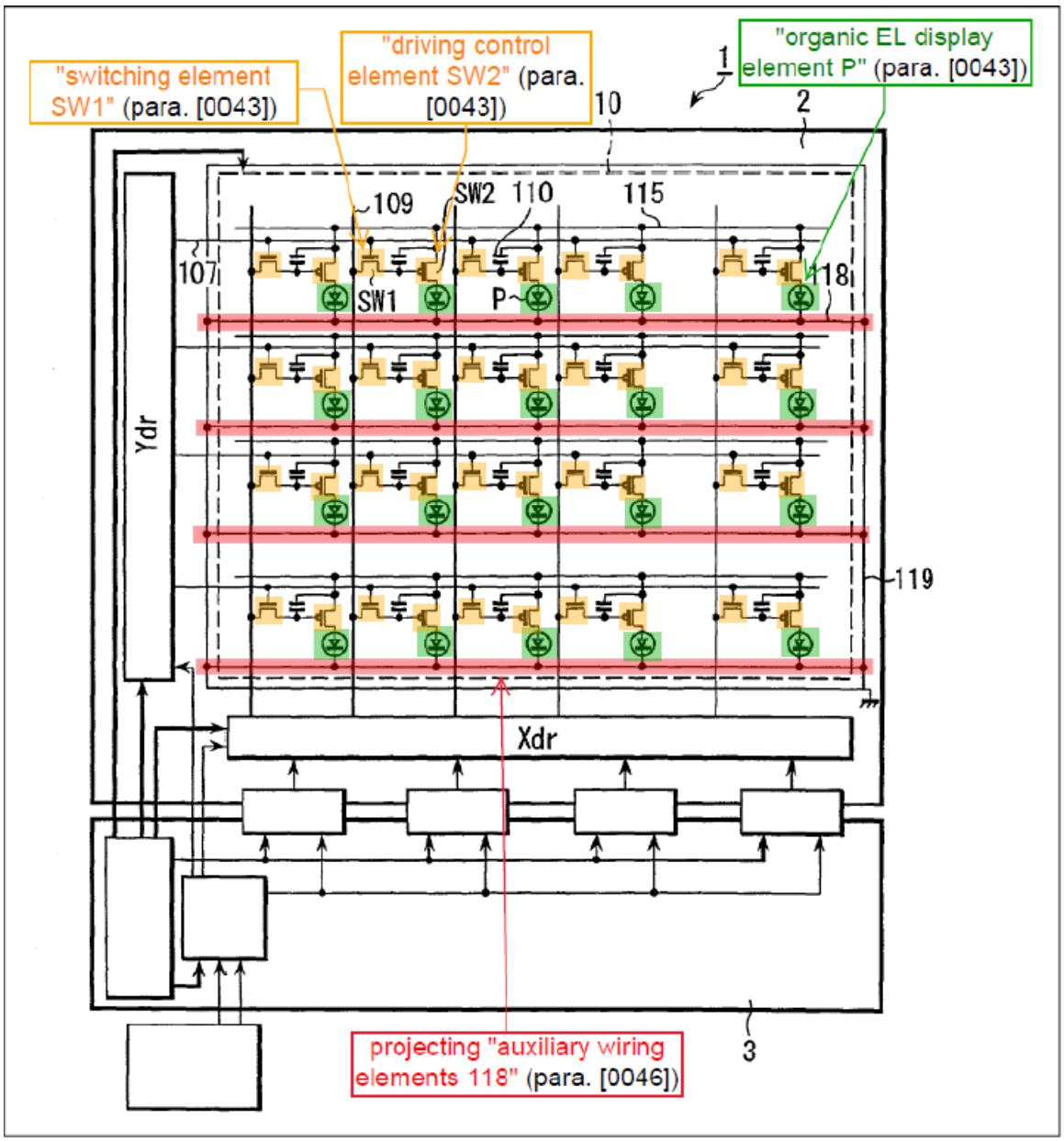
Petitioner replies that Kobayashi's auxiliary wiring elements meet the claimed limitation according to the district court's construction because they "extend beyond an outer surface of the transistor array substrate." Pet. Reply 14 (citing Ex. 1020, 18). Petitioner contends the relationship between Kobayashi's auxiliary wiring elements and the surface of the transistor array substrate is the same as the relationship between the '338 patent's common interconnections 91 and transistor array substrate surface – namely, that the projecting structure in each is "separated [from the surface] by an insulating film." *Id.* at 15; *see also id.* at 18 (asserting that because auxiliary wiring elements 118 are separated from the transistor array substrate by partition walls 120, the "auxiliary wiring elements 118 project from the surface . . . in exactly the same manner as common interconnections 91 of the '338 patent").

In its Sur-reply, Patent Owner again relies on its claim construction arguments in asserting that Kobayashi does not teach this limitation. PO Sur-reply 3–11.

As discussed above, we have construed "project from a surface of the transistor array substrate" to mean "extend beyond an outer surface of the transistor array substrate," consistent with the district court's construction, and we have not adopted Patent Owner's proposed further limitations to this construction. We find Petitioner has shown that Kobayashi teaches that its interconnections are formed to extend beyond the outer surface of the transistor substrate array. Specifically, Figure 7 of Kobayashi depicts auxiliary wiring elements 118 (i.e., interconnections) as extending beyond the outer surface of insulating layer 116 (i.e., transistor array substrate). *See* Ex. 1003, Fig. 7. Patent Owner's arguments that auxiliary wiring elements 118 are depicted as beginning above the surface of insulating layer 116 and that those wiring elements' extent in the vertical direction is small relative to their other dimensions (*see* PO Resp. 28–30) rely on a proposed claim construction that we have not adopted as discussed above. Accordingly, we determine Petitioner has persuasively shown Kobayashi's interconnections are formed to project from the surface of the transistor array substrate.

Claim 1 also recites "a plurality of pixel electrodes for the plurality of pixels, respectively, the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate." Ex. 1001, 24:22–25. Petitioner contends Kobayashi's "first electrodes 117" teach this limitation. *See* Pet. 46–49 (citing Ex. 1003 ¶¶ 44, 46, 51, 57, 71, 74, 90, 92, Fig. 7; Ex. 1018 ¶¶ 120–123). In particular, Petitioner contends Kobayashi discloses each "organic EL display element P comprises a first electrode 117 . . . [that] functions as the anode of the organic EL display element." *Id.* at 47 (citing Ex. 1003 ¶¶ 44, 51; Ex. 1018 ¶ 121) (internal quotations omitted). Petitioner further contends Kobayashi discloses auxiliary wiring elements 118 "are formed in

a lattice shape so as to surround the first electrode 117 of each display element P" and depicts such an arrangement in an annotated Figure 1 of Kobayashi as reproduced below. *Id.* at 47–48 (citing Ex. 1003 ¶¶ 46, 90, Fig. 1; Ex. 1018 ¶ 122).



Annotated Figure 1 of Kobayashi shows a plan view of Kobayashi's display device with Petitioner's annotations further identifying elements of that structure. *Id.* at 48; Ex. 1003 ¶ 29. Petitioner further contends Kobayashi

discloses that electrodes 117 are "disposed on" the surface of insulating layer 116. Pet. 48 (citing Ex. 1003 ¶ 74, Fig. 1; Ex. 1018 ¶ 123).

In its Patent Owner Response, Patent Owner contends Kobayashi's first electrodes 117 (i.e., pixel electrodes) are not "arrayed along" or "located between" auxiliary wiring elements 118 (i.e., interconnections) because "portions of the pixel electrodes are almost directly below the interconnections." PO Resp. 32 (citing Ex. 2005 ¶ 104). Patent Owner supports this position by referring to Figure 6 of the '338 patent and asserting: "This figure shows each of the sub-pixel electrodes 20a directly and entirely between interconnection 89 and the interconnection 90 on either side of it." *Id.* (citing Ex. 2005 ¶¶ 105–106).

Petitioner replies that Kobayashi "discloses a plurality of first electrodes 117 arrayed along and between the auxiliary wiring elements 118." Pet. Reply 19; *see also id.* at 20 (depicting annotated Figures 6A and 7 of Kobayashi, respectively depicting a top plan view and a side view of first electrodes and auxiliary wiring elements). Figure 6 A of Kobayashi is reproduced below.

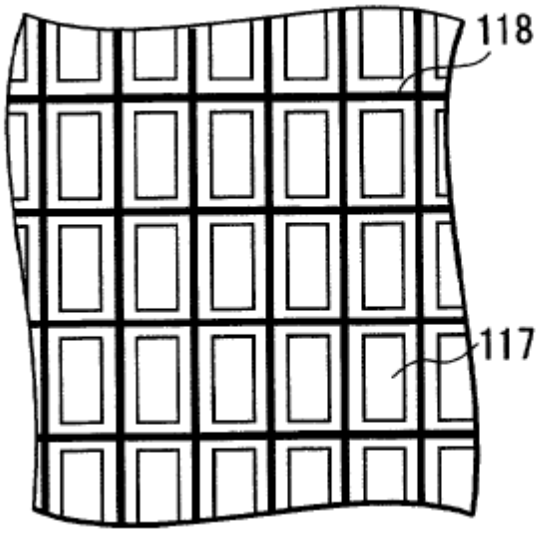


FIG. 6A

Figure 6A depicts a plan view showing first electrodes 117 and auxiliary wiring elements 118. Ex. 1003 ¶¶ 34, 53.

In its Sur-reply, Patent Owner responds that even if the first electrodes 117 were between the auxiliary wiring elements 118 of Kobayashi, one of ordinary skill in the art would not view structures 117 and 118 as being "arrayed along," since those structures are not coplanar and they do not share any overlapping layers. PO Sur-reply 13–14.

We find Petitioner has persuasively shown that Kobayashi teaches this limitation. Kobayashi states that the "auxiliary wiring elements 118 are formed in a lattice shape so as to surround the first electrode 117 of each display element P." Ex. 1003 ¶ 46. This lattice shape is shown in Figure 8 of Kobayashi as reproduced below.

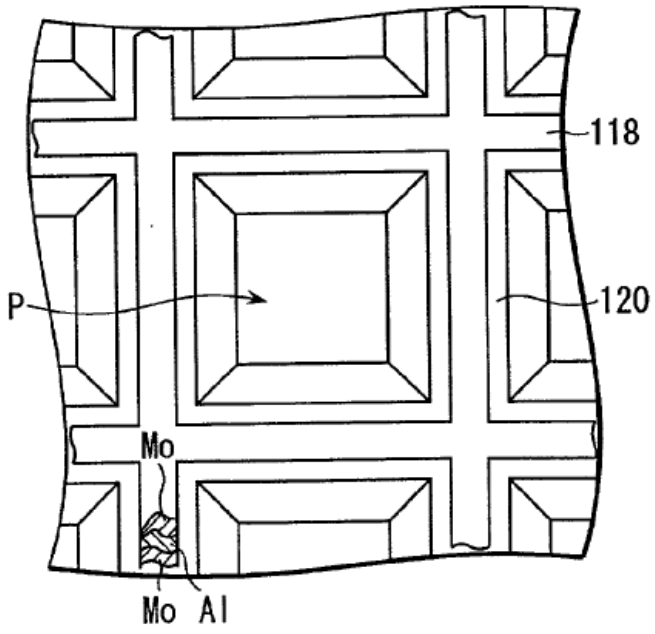


FIG. 8

Figure 8 of Kobayashi shows a plan view of the auxiliary wiring elements 118 surrounding pixels P. *Id.* ¶¶ 36, 90; *see id.* at Fig. 6A, ¶ 53. We agree

with Petitioner that this lattice structure shows that Kobayashi's auxiliary wiring elements 118 (interconnections) are arrayed along and located between Kobayashi's first electrodes 117 (pixel electrodes). Patent Owner's arguments to the contrary rely on claim constructions that we have not adopted as discussed above.

Accordingly, we determine Petitioner has shown Kobayashi teaches the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate.

Claim 1 also recites "a plurality of light-emitting layers formed on the pixel electrodes, respectively." Ex. 1001, 24:26–27. Petitioner contends "Kobayashi discloses 'organic light-emission layers 121' that are 'formed on'/'disposed on' each 'first electrode 117' in each 'display element P.'" Pet. 49 (citing Ex. 1003 ¶¶ 44, 79–80, 92; Ex. 1018 ¶ 125).

We determine Petitioner has shown Kobayashi teaches this limitation of claim 1. Kobayashi discloses that "an organic light-emission layer 121 functioning as a light active layer [] is disposed on the first electrode 117." Ex. 1003 ¶¶ 44, 92. We find these disclosures, cited by Petitioner, show that Kobayashi discloses "a plurality of light-emitting layers formed on the pixel electrodes, respectively" as recited in claim 1. We note that Patent Owner does not separately address this limitation (*see generally* PO Resp.; PO Sur-reply).

Claim 1 further recites "a counter electrode which is stacked on the light-emitting layers." Ex. 1001, 24:28–29. Petitioner contends "Kobayashi discloses a counter electrode (second electrode 12[2]) which is stacked on the light-emitting layers (organic light-emission layers 121)." Pet. 49–50 (citing Ex. 1003 ¶¶ 44, 51, 57, 80; Ex. 1018 ¶ 127).

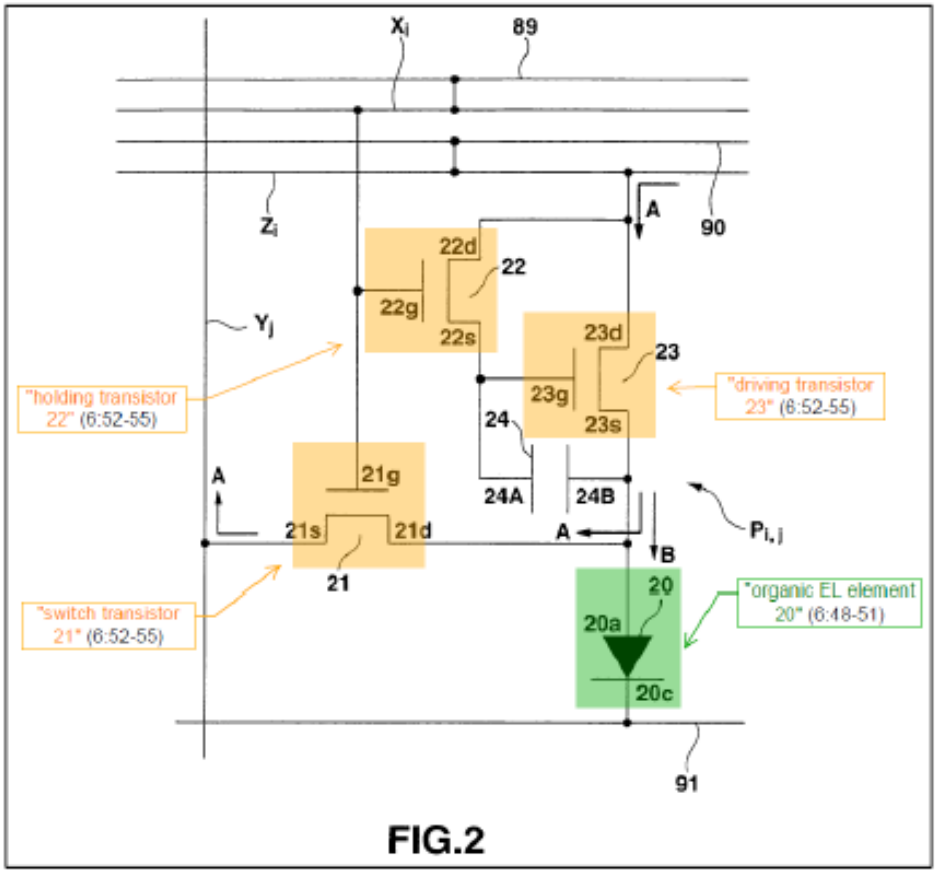
We determine Petitioner has shown Kobayashi teaches this limitation of claim 1. Kobayashi discloses that organic light-emission layer 121 is disposed on first electrode 117 and "a second electrode 122 disposed to be opposed to the first electrode 117 via the organic light-emission layer 121" functions as a cathode of first electrode 117 functioning as an anode. Ex. 1003 ¶¶ 44, 51, 80. We find these disclosures, cited by Petitioner, show that Kobayashi discloses "a counter electrode which is stacked on the light-emitting layers" as recited in claim 1. We note that Patent Owner does not separately address this limitation (*see generally* PO Resp.; PO Sur-reply).

Claim 1 also recites:

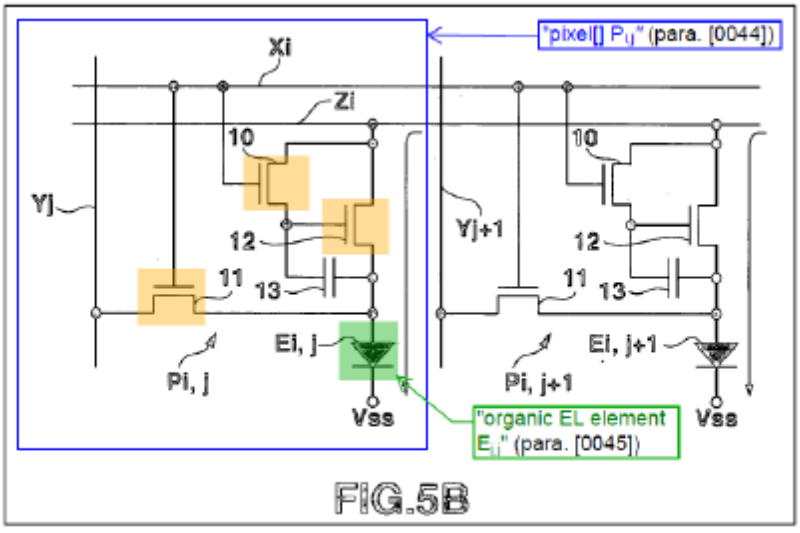
> wherein said plurality of transistors for each pixel include a driving transistor, one of the source and the drain of which is connected to the pixel electrode, a switch transistor which makes a write current flow between the drain and the source of the driving transistor, and a holding transistor which holds a voltage between the gate and source of the driving transistor in a light emission period.

Ex. 1001, 24:31–38. Petitioner contends the combination of Kobayashi and Shirasaki teaches this limitation. Pet. 50–57. Specifically, Petitioner contends "Kobayashi discloses that each pixel includes the claimed 'driving transistor' and 'switch transistor,' and it would have been obvious to further incorporate the claimed 'holding transistor' in view of Shirasaki," which "disclose[s] replacing a two-transistor-per-pixel circuit structure (as in Kobayashi) with a three-transistor-per-pixel circuit that includes each of the claimed 'driving transistor,' 'switching transistor,' and 'holding transistor.'" *Id.* at 50, 52.

Petitioner provides an annotated version of Figure 2 of the '338 patent and an annotated version of Figure 5B of Shirasaki, as reproduced below (*id.* at 52–53).



Ex. 1001 ('338 patent), Fig. 2 (annotated).



Ex. 1004 (Shirasaki), Fig. 5B (annotated).

The figures above, with annotations identifying certain elements and providing further citations to the '338 patent and Shirasaki, show the three-

transistor pixel circuits in the '338 patent and Shirasaki. As Petitioner notes (*id.* at 52), these circuits are substantially the same.

In explaining the combination of Kobayashi's and Shirasaki's teachings, Petitioner argues Shirasaki discloses "replacing a two-transistor-per-pixel circuit structure (as in Kobayashi) with a three-transistor-per-pixel circuit that includes each of the claimed 'driving transistor,' 'switching transistor,' and 'holding transistor.'" *Id.* at 52. Petitioner explains that Shirasaki teaches several advantages of replacing two-transistor pixel circuits with three-transistor pixel circuits, including "[c]urrent control [] performed by current values, not by voltage values. This suppresses the influence of variations in the voltage-current characteristic of the control system and allows the optical element to stably display images with desired luminance." *Id.* at 55 (citing Ex. 1004 ¶ 18; Ex. 1018 ¶ 138) (emphasis omitted). Another asserted advantage of Shirasaki is "that pixels stably display image with desired luminance in a display panel." *Id.* (citing Ex. 1004 ¶ 11; Ex. 1018 ¶ 139). Petitioner also notes Shirasaki teaches advantages of three-transistor pixel circuits over pixel circuits with four or more transistors, including lower power consumption and improved apparent brightness. *Id.* at 55 n.5 (citing Ex. 1004 ¶¶ 9, 12, 19–20; Ex. 1018 ¶ 140).

Discussing the reasonable expectation of success, Petitioner contends that Shirasaki "expressly discloses that its three-transistor pixel circuit is meant to replace the two-transistor pixel circuit found in 'conventional light emitting element display' devices." *Id.* at 56 (citing Ex. 1004 ¶¶ 2–8, 13–19). Petitioner further contends that Kobayashi and Shirasaki come from the same field of endeavor of "active matrix organic light-emitting diode display panels featuring thin-film transistor arrays." *Id.* (citing Ex. 1003 ¶ 2; Ex. 1004 ¶¶ 41, 43; Ex. 1018 ¶¶ 142–143). Petitioner also contends that a

person of ordinary skill in the art would have recognized Shirasaki's three-transistor circuit could have been implemented "without altering any of the layers above the transistor array substrate in Kobayashi's layered OLED [organic light emitting diode] structure." *Id.* & n.6 (citing Ex. 1018 ¶ 146) (discussing implementing Shirasaki's three-transistor circuit would require "changing the photomasks used to fabricate the TFT array and relocating the contact holes through Kobayashi's insulating layer 116" and that such steps "were routine and predictable manufacturing steps involved during the fabrication of every OLED display panel").

Petitioner further points to disadvantages of two-transistor circuits discussed in Shirasaki. *Id.* at 53–54 (quoting Ex. 1004 ¶ 7 ("difficult to display images with a desired luminance tone for long time periods"; "no accurate tone control"; "difficult to make the characteristics of the transistors [] of the individual pixels uniform"). Petitioner also argues Shirasaki discloses advantages to replacing a two-transistor circuit with Shirasaki's three-transistor circuit. *Id.* at 54–55 (quoting Ex. 1004 ¶¶ 18 ("Current control is thus performed by the current values, not by voltage values. This suppresses the influence of variations in the voltage-current characteristic of the control system and allows the optical element to stably display images with desired luminance."), 11 ("[O]ne advantage of the present invention is that pixels stably display image with desired luminance in a display panel.")).

In its Patent Owner Response, Patent Owner asserts that a person of ordinary skill in the art would not have been motivated to replace Kobayashi's two-transistor pixel circuit with Shirasaki's three-transistor pixel circuit. PO Resp. 17–26. First, Patent Owner asserts that Kobayashi and Shirasaki are directed to different problems. *Id.* at 17–19. In particular,

Patent Owner contends that Kobayashi is aimed at reducing non-uniformity in electrode voltage (i.e., display quality), specifically at the edges of a display, whereas Shirasaki is aimed at addressing aging transistors, which decreases luminescence over time. *Id.* (Ex. 1003 ¶ 6; Ex. 1004 ¶ 7). Patent Owner contends the solution Kobayashi provides is a lattice structure for electrodes that increases voltage uniformity and increases display quality. *Id.* at 18 (citing Ex. 1018 ¶¶ 118, 122). Patent Owner also contends that "[t]he problem addressed by Kobayashi has nothing to do with the transistors in the pixel circuit," such as "[v]ariation in transistor threshold voltage, channel resistance, ageing, and temperature." *Id.* Regarding Shirasaki, Patent Owner asserts that "[b]oth the purported solution and approach of Shirasaki involves current-written pixel circuits, and not voltage-written circuits as in Kobayashi." *Id.* at 19.

Patent Owner also contends that Kobayashi and Shirasaki being directed broadly to improvements in OLED displays or TFT pixels is insufficient to show a motivation to combine. *Id.* at 19–20. In particular, Patent Owner asserts that "Petitioner fails to address the differences in proposed solutions between Kobayashi and Shirasaki or the differences between a voltage-written approach versus [a] current-written approach." *Id.* at 20.

Patent Owner further contends that Petitioner mischaracterizes Shirasaki's teachings. *Id.* at 20–23. Specifically, Patent Owner asserts that Shirasaki attempts to improve upon art as using voltage-written circuits (i.e., voltage driving method) and that it is "impossible to apply to amorphous silicon transistors" such as in background prior art circuits. *Id.* at 21 (citing Ex. 1004 ¶¶ 3, 6, 8). Regarding Shirasaki's discussion of the number and materials of transistors, Patent Owner asserts that Shirasaki discusses non-

voltage-driven circuits with too many transistors (that make the upper surface of the substrate uneven) and teaches pairing down the number of transistors within the current-driven circuits. *Id.* (citing Ex. 1104 ¶ 9). To the extent Shirasaki teaches improvement over two-transistor circuits, Patent Owner contends those prior art devices discussed by Shirasaki are limited to using amorphous silicon transistors and that there is nothing disclosed in Shirasaki about adding a transistor for the circuits with polysilicon transistors such as those used in Kobayashi. *Id.* at 22 (citing Ex. 1004 ¶¶ 3, 8–9, 112).

Finally, Patent Owner contends that Petitioner fails to show how a person of ordinary skill in the art would have modified Kobayashi with Shirasaki and how they would have done so with a reasonable expectation of success. *Id.* at 23–26. In particular, Patent Owner asserts that the Petitioner's description of the modification is an unexplained wholesale substitution, and the details of the required changes of how "the existing transistors and other elements are connected, operate, and are driven" are not addressed. *Id.* at 23. As an example, Patent Owner highlights the differences between the scan drivers, data line, and switch transistor of Kobayashi as being geared towards applying voltages and carrying insignificant current (i.e., voltage-driven) versus Shirasaki's current-driven components. *Id.* at 24–25. Patent Owner also asserts that the Petition "does not address a 'write current' in the context of the proposed combination of Kobayashi and Shirasaki" and asserts that "leaving the alleged 'write current' from Kobayashi unmodified [in replacing the two-transistor circuit of Kobayashi with the three-transistor circuit of Shirasaki] would result in a non-functioning device." *Id.* at 25–26.

In its Reply, Petitioner stresses the advantages expressly taught by Shirasaki's three-transistor circuit include "suppress[ing] the influence of variations in voltage-current characteristic of control system and allow[ing] the optical element to stably display images with desired luminance." Pet. Reply 5–6 (citing Ex. 1004 ¶¶ 11, 18; Ex. 1018 ¶¶ 138–139). Petitioner addresses Patent Owner's arguments that Kobayashi and Shirasaki are "directed to different problems" and asserts (1) that such an argument is legally misplaced as not focusing on the motivation to combine, and (2) that "Shirasaki and Kobayashi are both directed to improving image characteristics in active matrix OLED displays, lowering power consumption, and extending [the display's] useful life." *Id.* at 6 (citing Ex. 1003 ¶¶ 83–84, 104; Ex. 1004 ¶¶ 19, 94).

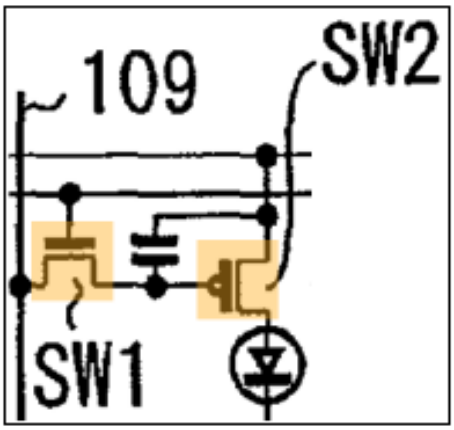
Petitioner also asserts that because Shirasaki discusses improving on conventional two-transistor voltage-driven circuits and also discusses problems with using four or more transistors per circuit, Shirasaki expressly teaches replacing a two-transistor voltage-drive circuit with a three-transistor current-drive circuit. *Id.* at 7 (citing PO Resp. 21–22; Ex. 1004 ¶¶ 4–6, 9). Petitioner further contends Shirasaki discusses the problems associated with, and overcoming, two-transistor polysilicon transistors. *Id.* at 8 (citing Ex. 1004 ¶ 7; Ex. 1025, 38:3–8). Even so, Petitioner contends Shirasaki provides "that *either* amorphous silicon *or* polysilicon transistors may be used." *Id.* (citing Ex. 1004 ¶ 112; Ex. 1025, 41:10–42:18).

Petitioner further explains the reasonable expectation of success. *Id.* at 9–14. Petitioner asserts that replacing Kobayashi's two-transistor circuit with Shirasaki's three-transistor circuit "would simply require changing the photomasks used to fabricate the transistor array and relocating certain contact holes," and that such techniques "were routine and predictable

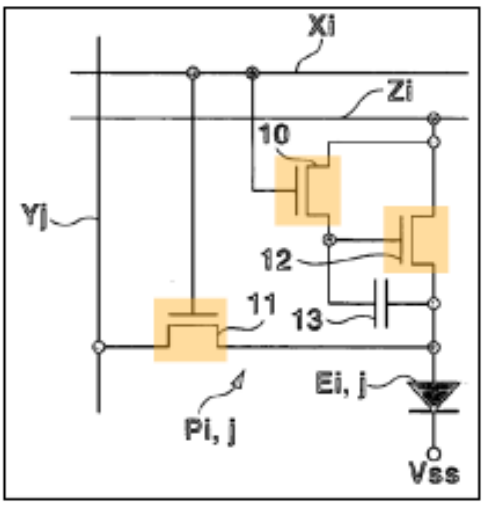
manufacturing steps [] which [Patent Owner] does not dispute." *Id.* at 9 (citing Pet. 57 & n.6; Ex. 1018 ¶ 146). Petitioner refutes that the proposed modification is an unexplained wholesale substitution by explaining how Shirasaki teaches the technical details of implementing Shirasaki's three-transistor circuit. *Id.* at 10–12 (citing Ex. 1004 ¶¶ 34, 68–88, Figs. 5a, 7; Ex. 1025, 44:10–14, 57:3–59:15). In particular, Petitioner explains that Shirasaki "details how to connect the transistors to one another," "how to operate the circuit," and "details the driving circuitry," including shift registers and sink drivers. *Id.* (citing Ex. 1004 ¶¶ 34, 68–88, Figs. 5a, 7). Regarding Patent Owner's arguments about Kobayashi's unmodified "write current," Petitioner asserts that replacing the two-transistor circuit of Kobayashi with the three-transistor circuit of Shirasaki entails replacing Kobayashi's write current with Shirasaki's memory current. *Id.* at 13–14 (citing Paper 7, 3 ("Pet. Supp. Br.") (citing Ex. 1004 ¶¶ 72, 84; Ex. 1001, 15:34–37)).

We have considered the parties' arguments and evidence on this issue as detailed above, and we find Petitioner's contentions persuasive. As Petitioner asserts, "[Patent Owner] does not dispute that Shirasaki meets the circuit structure recited in [claim 1]." *Id.* at 4–5. Thus, the issue here concerns the motivation to combine, namely, the motivation "to replace Kobayashi's two-transistor voltage-driven pixel circuit [as depicted in annotated Figure 1 of Kobayashi below] with Shirasaki's three-transistor current-driven pixel circuit [as depicted in annotated Figure 5B of Shirasaki below]." Pet. 53–56; Pet. Reply 5; *see also* Tr. 14:7–15 (confirming the proposed modification "is essentially replacing Kobayashi's two-transistor circuit with Shirasaki's three-transistor circuit, not . . . a picking and choosing of components").

An annotated excerpt of Figure 1 of Kobayashi and annotated Figure 5B of Shirasaki are reproduced below.



Kobayashi's 2-Transistor Circuit
Ex. 1003, Fig. 1 (annotated excerpt)



Shirasaki's 3-Transistor Circuit
Ex. 1004, Fig. 5B (annotated)

The annotated excerpt of Figure 1 of Kobayashi depicts its two transistor circuit, and the annotated Figure 5B of Shirasaki depicts its three transistor circuit, with the transistors highlighted in each.

We agree with Petitioner that Shirasaki provides an express teaching for the proposed modification, namely, to "suppress[] the influence of variations in voltage-current characteristic of control system and allow[] the optical element to stably display images with desired luminance." Pet. Reply 5–6 (citing Ex. 1004 ¶¶ 11, 18; Ex. 1018 ¶¶ 138–139). We are persuaded that Shirasaki improves upon "conventional" two-transistor circuits and "teaches benefits of replacing a two-transistor voltage-drive circuit with a three-transistor current-drive circuit." *Id.* at 7 (citing Ex. 1004 ¶¶ 4–6).

We are unpersuaded that a person of ordinary skill in the art would not have been motivated to modify Kobayashi in view of Shirasaki because the two are allegedly directed to different problems. We agree with

Petitioner that "Shirasaki and Kobayashi are both directed to improving image characteristics in active matrix OLED displays, lowering power consumption, and extending [the display's] useful life." *Id.* at 6 (citing Ex. 1003 ¶¶ 83–84, 104; Ex. 1004 ¶¶ 19, 94). Kobayashi discloses increasing luminance of the display while also lowering power consumption, and Shirasaki also discusses increasing the apparent brightness of the display and lowering power consumption. Ex. 1003 ¶¶ 83–84, 104; Ex. 1004 ¶¶ 19, 94. Petitioner is also correct that "the motivation to combine inquiry focuses on whether one of ordinary skill would have been motivated to combine the teachings of both references as a whole, not whether the problems solved by the prior art are the same." Pet. Reply 6 (citing *Google LLC v. Virentem Ventures, LLC*, No. IPR2019-01247, 2020 WL 1140494, at *12 (PTAB Mar. 9, 2020)). Thus, we determine a person of ordinary skill in the art would have recognized the similar nature of both Kobayashi's and Shirasaki's teachings and, also, would not have been dissuaded from combining their teachings even if there are some particular differences in the specific problems addressed.

We also agree with Petitioner that Shirasaki discusses improving on conventional two-transistor circuits where the driving method is called a voltage driving method. Pet. Reply 7 (citing Ex. 1004 ¶¶ 4, 6). We further agree with Petitioner that Shirasaki discusses non-voltage-driven circuits made up of four or more transistors in one pixel and that there are various disadvantages to having too many transistors in such an arrangement. *Id.* (citing Ex. 1004 ¶ 9). For example, when too many transistors are formed on a substrate, the light emission life of the pixel shortens and "the fabrication yield lowers exponentially." Ex. 1004 ¶ 9. Regarding the materials of the transistors, we agree with Petitioner that Shirasaki discusses

improving on channel layers of transistors made of polysilicon. Pet. Reply 8 (citing Ex. 1004 ¶ 7). Shirasaki discusses that if polysilicon is used in the channel layers of the transistors, "the channel resistances depend upon the numbers of grain boundaries as the interfaces between adjacent crystal grains in these channel layers," and "[a]s a consequence, no accurate tone control can be performed," i.e., there are unintended variations in the display characteristics of individual pixels in a single panel. Ex. 1004 ¶ 7. Even so, Shirasaki leaves open the possibility of using amorphous silicon or polysilicon in the thin film transistors. *Id.* ¶ 112. Thus, we find Shirasaki teaches improvements on conventional pixel circuits using both two transistors and four or more transistors, and accounts for different materials of the transistors within these teachings.

Regarding reasonable expectation of success, we agree with Petitioner's explanation that the required manufacturing changes of "changing the photomasks used to fabricate the TFT array and relocating the contact holes through Kobayashi's 'insulating layer 116' that connect the TFT array to the OLED elements, [] were routine and predictable manufacturing steps." Pet. 57 n.6 (citing Ex. 1018 ¶ 146 (citing Ex. 1005, 14:29–15:2, 15:25–28, 16:8–10)); Pet. Reply 9. In supporting his opinion that these were routine and predictable manufacturing steps, Dr. Fontecchio relies on Childs as an example showing that the techniques were known to those of skill in the art at the relevant timeframe. Ex. 1018 ¶ 146 (citing Ex. 1005, 14:29–15:2). We also determine that Petitioner sufficiently explains how to connect, operate, and drive the three-transistor circuit of Shirasaki as substituted for the two-transistor circuit of Kobayashi. Pet. Reply 10–11 (citing Ex. 1004 ¶¶ 68, Fig. 5a (describing and depicting how to connect the transistors of the circuit to one another and the associated signal lines), 69–

88 (discussing how to operate the three-transistor circuit of Shirasaki), 69–70, 72 (detailing the driving circuitry necessary to implement a three-transistor current-drive circuit); Ex. 1025, 44:10–14, 57:3–59:15).

Regarding Patent Owner's assertions that Petitioner fails to account for the unmodified "write current" of Kobayashi, Petitioner notes that the modification of substituting Kobayashi's two-transistor circuit with Shirasaki's three-transistor circuit entails incorporating the write current (memory current) of Shirasaki's circuit. *Id.* at 12–13 (citing Pet. 55; PO Resp. 25–26). In particular, Petitioner notes that "the 'memory current' **α** that flows in Shirasaki's three-transistor circuit when 'transistor 11' (the claimed 'switch transistor') 'is turned on,' . . . is the same as 'pull-out current' A shown in annotated Fig. 2 of the '338 patent." *Id.* at 13–14 (citing Pet. Supp. Br. 3 (citing Ex. 1004 ¶¶ 72, 84, Fig. 5a; Ex. 1001, 15:34–37, Fig. 2)). Thus, we determine that Petitioner has sufficiently shown a reasonable expectation of success for its proposed modification.

For the reasons discussed above, we determine Petitioner has shown a person of ordinary skill in the art would have been motivated to replace Kobayashi's two-transistor circuit with Shirasaki's three-transistor circuit to include a switch transistor that makes a write current flow between the drain and the source of the driving transistor. In sum, for the reasons discussed above, we determine Petitioner has shown by a preponderance of the evidence that claim 1 is unpatentable as obvious over Kobayashi and Shirasaki.

Dependent claims 2, 5, 6, and 9–11

Petitioner also has shown the additional limitations of dependent claims 2, 5, 6, and 9–11 are taught in Kobayashi or would have been obvious

in light of Kobayashi's teachings. Pet. 58–62. Claim 2 depends from independent claim 1 and additionally recites:

> wherein said plurality of interconnections include at least one of a feed interconnection connected to the other of the source and the drain of at least one of the driving transistors, a select interconnection which selects at least one of the switch transistors, and a common interconnection connected to the counter electrode.

Ex. 1001, 24:39–44. Petitioner contends a person of ordinary skill in the art "would have understood this claim to require that the plurality of interconnections include at least one of the three types of claimed interconnections . . . as opposed to requiring all three types of claimed interconnections, as recited by dependent claim 4." Pet. 58 (citing Ex. 1018 ¶ 147). Petitioner further contends that Kobayashi teaches common interconnections connected to the counter electrode. *Id.* (citing Ex. 1018 ¶ 148). We are persuaded because Kobayashi states: "the auxiliary wiring element 118 is electrically connected to the second electrode 122" to reduce the resistance of the entire light-emission-side electrode and suppress display non-uniformity much like the common interconnection 91 of the '338 patent "reduce[s] the sheet resistance of the cathode electrode." Ex. 1003 ¶¶ 62, 83; Ex. 1001, 14:8–19. We note that Patent Owner does not separately address this claim (*see generally* PO Resp.; PO Sur-reply).

Claim 5 depends from independent claim 1 and additionally recites "wherein said plurality of pixels include a red pixel, a green pixel, and a blue pixel." Ex. 1001, 24:53–54. Petitioner contends Kobayashi discloses "its plurality of pixels include red pixels, green pixels, and blue pixels." Pet. 58. We are persuaded because Kobayashi states: "organic EL panel 2 comprises three kinds of display elements P, which respectively emit red, green and

blue light." Ex. 1003 ¶ 41; *see also id.* ¶¶ 44, 56, 79 (discussing the different colors of display elements/pixels P). We note that Patent Owner does not separately address this claim (*see generally* PO Resp.; PO Sur-reply).

Claim 6 depends from dependent claim 5 and additionally recites "wherein said plurality of pixels comprises a plurality of sets each including the red pixel, green pixel, and blue pixel arrayed in an arbitrary order." Ex. 1001, 24:55–58. Petitioner contends a person of ordinary skill in the art "would have recognized that Kobayashi's pixels comprise a plurality of sets each including the red pixel, the green pixel, and the blue pixel arrayed in an arbitrary order." Pet. 59. We are persuaded. For example, Kobayashi states: "organic EL panel 2 comprises three kinds of display elements P, which respectively emit red, green and blue light" and that "organic light-emission materials corresponding to red (R), green (G) and blue (B) are successively jetted out by an ink jet method," thus forming organic light-emission layers 121 of the respective colors. Ex. 1003 ¶¶ 41, 79; Ex. 1018 ¶¶ 151–152). We note that Patent Owner does not separately address this claim (*see generally* PO Resp.; PO Sur-reply).

Claim 9 depends from independent claim 1 and additionally recites "wherein at least one of the interconnections has a resistivity of 2.1 to 9.6 μΩcm." Ex. 1001, 24:64–65. Petitioner contends Kobayashi discloses "it is preferable, in particular, that the auxiliary wiring element" (i.e., interconnection) "be formed of a conductive material with a resistivity of $1x10^{-6}$ Ωcm to $6x10^{-6}$ Ωcm." Pet. 60 (citing Ex. 1003 ¶ 49). We are persuaded. For example, Kobayashi states: the "resistivity of the auxiliary wiring element 118 . . . is about 3 μΩcm" – within the claimed range. Ex. 1003 ¶ 89; *see also id.* ¶ 49, Fig. 4 (providing electrical resistivity of

typical metal materials chose for auxiliary wiring element 118). We note that Patent Owner does not separately address this claim (*see generally* PO Resp.; PO Sur-reply).

Claim 10 depends from independent claim 1 and additionally recites "wherein said plurality of interconnections are formed from a conductive layer that is different from a layer forming the source and the drain of each of the transistors and a layer forming the gate of the transistors." Ex. 1001, 24:66–25:3. Petitioner contends Kobayashi discloses the auxiliary wiring element 118 being formed from "metal materials" and the transistors' source, drain, and gate formed from polysilicon, and in the alternative, discloses the auxiliary wiring elements 118 formed of a different conductive layer above the insulating layer 116 whereas the source, drain, and gate of the transistors are "formed under insulating layer 116." Ex. 1003 ¶¶ 49, 65–69, Fig. 7; Ex. 1018 ¶ 156. We find these contentions are supported by the cited disclosures. We note that Patent Owner does not separately address this claim (*see generally* PO Resp.; PO Sur-reply).

Claim 11 depends from independent claim 1 and additionally recites "wherein said plurality of interconnections are formed from a conductive layer different from a layer forming the pixel electrodes." Ex. 1001, 25:4–6. Petitioner contends auxiliary wiring elements 118 are formed on a layer on top of partition walls 120, which are themselves on top of first electrodes 117. Ex. 1003 ¶ 92, Fig. 7; Ex. 1018 ¶ 158. We find these contentions are supported by the cited disclosures. We note that Patent Owner does not separately address this claim (*see generally* PO Resp.; PO Sur-reply).

For the reasons discussed above, we determine Petitioner has demonstrated by a preponderance of the evidence that claims 1, 2, 5, 6, and 9–11 would have been obvious over Kobayashi and Shirasaki.

E. Asserted Obviousness over Childs and Shirasaki

1. Childs (Ex. 1005)

Childs describes an active-matrix electroluminescent display (AMELD) having an array of pixels on a circuit substrate. Ex. 1005, 6:23–25. Figure 1, reproduced below, shows an array of four pixels, the pixels having an exemplary pixel circuit configuration. *Id.* at 5:3–5.

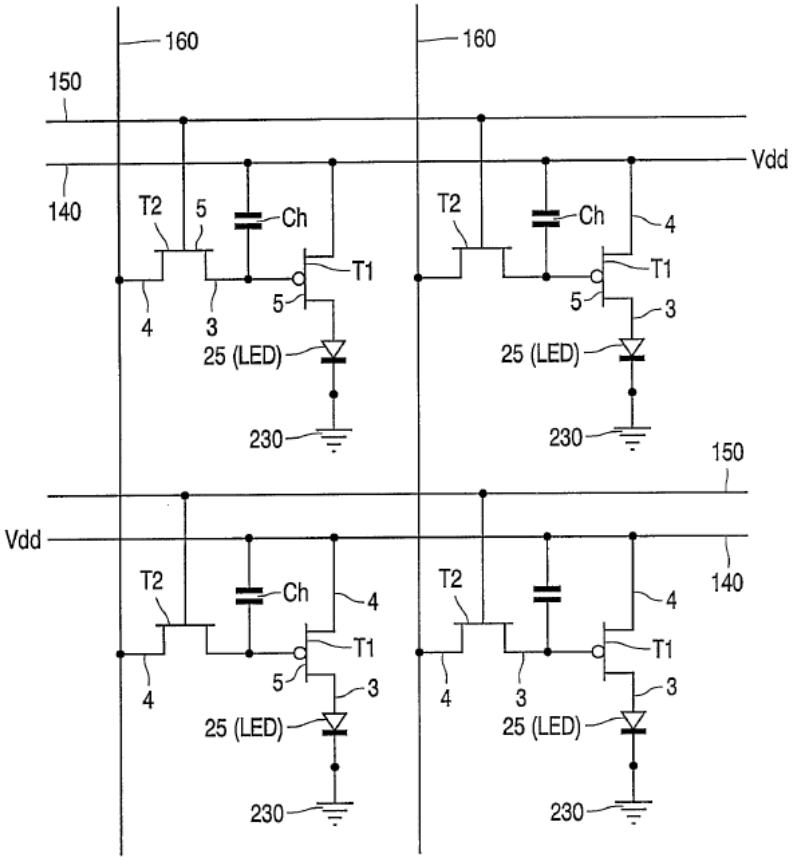


FIG. 1

As shown in Figure 1, for each respective pixel circuit, "pixel 200 comprises a current-driven electroluminescent display element 25," e.g., light-emitting diode (LED) of organic semiconductor material; two transistors, i.e., drive element T1 and addressing element T2; and a holding

capacitor Ch. *Id.* at 7:3–6, 10–14, 25. In the pixel circuit, "LED 25 is connected in series with a drive element T1 (typically a [thin-film transistor (TFT)]) between two voltage supply lines 140 and 230" such that "[l]ight emission from the LED 25 is controlled by the current flow through the LED 25, as altered by its respective drive TFT T1." *Id.* at 7:12–17.

Furthermore, "[e]ach row of pixels is addressed in turn in a frame period by means of a selection signal" which "turns on the addressing TFT T2, [and] so loading the pixels of that row with respective data signals from the column conductors 160." *Id.* at 7:18–22. The "data signal is maintained on [TFT T2's] gate 5 by a holding capacitor Ch." *Id.* at 7:24–25. Accordingly, "the drive current through the LED 25 of each pixel 200 is controlled by the driving TFT T1 based on a drive signal applied during the preceding address period and stored as a voltage on the associated capacitor Ch." *Id.* at 7:26–29.

The aforementioned pixel circuitry is constructed over an insulating layer. *Id.* at 7:31–8:2. The layering of pixel circuitry elements is shown in Figure 2, reproduced below.

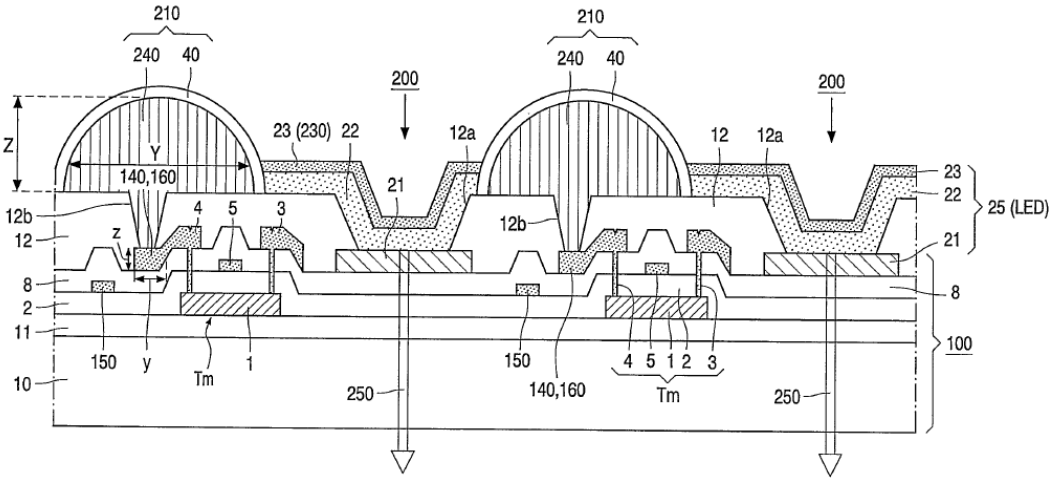


FIG. 2

As shown in Figure 2, TFTs Tm and Tg are layered over insulating glass base 10 and surface-buffer layer 11. *See id.* at 7:32–8:8. Layered over electrodes 3, 4 of the TFTs are "conductor lines 140, 150 and 160," as described above. *Id.* at 8:8–13. And still further layered over TFTs Tm and Tg is LED 25, which "comprises a light-emitting organic semiconductor material 22 between a lower electrode 21 and an upper electrode 23." *Id.* at 8:16–17.

2. Analysis

Petitioner contends claims 1–3 and 5–13 are unpatentable as obvious over Childs and Shirasaki. Pet. 63–92; Pet. Reply 21–32. We have reviewed the evidence and arguments provided by the parties and are persuaded that Petitioner has demonstrated by a preponderance of the evidence that claims 1–3 and 5–13 are unpatentable as obvious over Childs and Shirasaki.

Claim 1

Claim 1 recites "[a] display panel." Ex. 1001, 24:14. Petitioner contends Childs teaches this limitation. Pet. 64. In particular, Petitioner contends Childs discloses "an active-matrix electroluminescent display (AMELD) device." *Id.* (citing Ex. 1005, 6:23–25; Ex. 1018 ¶ 162).

We determine Petitioner has shown Childs teaches this limitation of claim 1. Childs discloses the embodiments of the device of Figures 1–3 is an "active-matrix electroluminescent display (AMELD) device." Ex. 1005, 6:23–25. We find this disclosure, cited by Petitioner, shows that Childs discloses "[a] display panel" as recited in claim 1. We note that Patent Owner does not separately address this limitation (*see generally* PO Resp.; PO Sur-reply).

Claim 1 recites "a transistor array substrate which includes a plurality of pixels and comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain." Ex. 1001, 24:15–18. Petitioner contends Childs teaches this limitation. Pet. 64–68 (citing Ex. 1005, 6:23–27, 7:10–8:27, 10:25–27, 14:30–32, Fig. 2; Ex. 1018 ¶¶ 165–170). In particular, Petitioner contends "Childs describes the layered structure of 'circuit substrate 100,' which extends from 'insulating glass base 10' through 'insulating layers' 11, 2 and 8 and 'planar insulating layer 12.'" *Id.* at 64 (citing Ex. 1005, 6:23–25, 7:31–8:27, 14:30–32). Petitioner provides an annotated version of Figure 2 of Childs and also relies on the testimony of Dr. Fontecchio in support of the assertion that a person of ordinary skill in the art "would have recognized that the layered structure of Child's 'circuit substrate 100' [extending from insulating glass base 10 through planar insulating layer 12] comprises a transistor array substrate." *Id.* at 64–65 (citing Ex. 1005, Fig. 2; Ex. 1018 ¶¶ 165–166) (internal quotations omitted). Petitioner further contends Childs' display device "comprises an array of pixels 200 on a circuit substrate 100" as depicted in Figure 2 of Childs. *Id.* at 65 (citing Ex. 1005, 6:23–27, Fig. 2; Ex. 1018 ¶ 168). Petitioner also contends that "[e]ach pixel 200 comprises" both a drive thin film transistor (TFT) T1 and an addressing TFT T2, with each TFT including "source and drain regions," "gate electrode 5," and "gate dielectric layer 2" (gate insulating film). *Id.* at 66–67 (citing Ex. 1005, 7:10–30, 8:3–15, Fig. 1; Ex. 1018 ¶¶ 169–170).

We determine Petitioner has shown Childs teaches this limitation of claim 1. Childs discloses "an array of pixels 200 on a circuit substrate 100 with matrix addressing circuitry" and also depicts each pixel area of an AMELD display included transistors T1, T2 (examples Tm and Tg as

depicted in Figures 2–3). Ex. 1005, 6:23–25, 7:10–30, 8:3–15, Figs. 1–3. Childs further discloses each transistor example Tm, Tg contains a gate electrode 5, gate dielectric layer 2, and source and drain regions. *Id.* at 8:3–15. We find these disclosures, cited by Petitioner, show that Childs discloses "a transistor array substrate which includes a plurality of pixels and comprises a plurality of transistors for each pixel, each of the transistors including a gate, a gate insulating film, a source, and a drain" as recited in claim 1. We note that Patent Owner does not separately address this limitation (*see generally* PO Resp.; PO Sur-reply).

Claim 1 further recites "a plurality of interconnections which are formed to project from a surface of the transistor array substrate, and which are arrayed in parallel to each other." Ex. 1001, 24:19–21. Petitioner contends "Childs discloses that its 'physical barriers 210' 'are constructed with conductive barrier material 240 that is used as an interconnection,'" and "conductive barriers 240 are 'deposited on the insulating layer 12,' project from the surface of insulating layer 12 (i.e., from the claimed 'surface of the transistor array substrate'), and are arrayed in parallel to each other." Pet. 68–69 (citing Ex. 1005, 6:25–29, 9:3–11, 9:20–29, 15:9–23, Fig. 2; Ex. 1018 ¶¶ 172–173).

We determine Petitioner has shown Childs teaches this limitation of claim 1. Childs discloses "[p]hysical barriers 210 are constructed with conductive barrier material 240 that is used as an interconnection," and barriers 210 "are connected to and/or from one or more circuit elements of the circuit substrate 100," and such barriers appear to be arranged in parallel. Ex. 1005, 6:25–29, 9:20–29, Figs. 1–2. We find these disclosures, cited by Petitioner, show that Childs discloses "a plurality of interconnections which are formed to project from a surface of the transistor array substrate, and

which are arrayed in parallel to each other" as recited in claim 1. We note that Patent Owner does not separately address this limitation (*see generally* PO Resp.; PO Sur-reply).

Claim 1 also recites "a plurality of pixel electrodes for the plurality of pixels, respectively, the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate." Ex. 1001, 24:22–25. Petitioner contends Childs teaches this limitation. Pet. 69–75 (citing Ex. 1005, 7:10–12, 8:3–27, 14:29–5:2, Fig. 2; Ex. 1018 ¶¶ 176–180, 184, 188–191). In particular, Petitioner contends Childs teaches lower electrodes 21 for each pixel, which are arrayed along and between conductive barriers 240 (i.e., "the interconnections") and formed on insulating layer 8 and exposed in connection windows 12a. *Id.* at 70–71 (citing Ex. 1005, 8:3–27, Fig. 2; Ex. 1018 ¶¶ 177–178).

Additionally, Petitioner provides an alternative explanation as to how this limitation would have been obvious even if Childs' insulating layer 8 is not on the surface of the transistor array substrate. *See id.* at 71–75. Petitioner asserts that "to the extent that there is any question whether lower electrode 21 of Childs is arrayed 'on the surface of the transistor array substrate' (e.g., because lower electrode 21 is not on top of the insulating layer 12 which covers aluminum electrodes 3 and 4), it would have been obvious to form lower electrode 21 on the surface of an insulating layer that covers these electrodes 3 and 4" and such a modification would have been straightforward. *Id.* at 71–72 (citing Ex. 1018 ¶ 179).

First, Petitioner contends one option for this modification would have been "to form an additional transparent insulating layer on top of aluminum electrodes 3 and 4, with lower electrode 21 then formed on top of that

additional insulating layer (i.e., on the surface of the transistor array substrate)." *Id.* at 72. In the alternative, Petitioner contends that "lower electrode 21 may be formed on top of planar insulating layer 12 (instead of on the exposed surface of insulating layer 8)" and that such a modification would have been a mere reordering of the steps of Childs's fabrication process. *Id.* at 72–73 & nn.7–8 (citing Ex. 1018 ¶ 180). Petitioner asserts, and Dr. Fontecchio testifies, that "forming the pixel electrodes . . . on top of an insulating layer that covers the metal source and drain electrodes . . . was a well-known and obvious manufacturing technique at the time of the alleged invention of the '338 patent." *Id.* at 73. In support, Petitioner points to other prior art showing this manufacturing technique such as Kobayashi and Park (Ex. 1014) and also to *KSR* for the rationale that "where . . . there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *Id.* at 73–74 (citing Ex. 1003; Ex. 1009; Ex. 1014; *KSR*, 550 U.S. at 421).

Again referring to the teachings of other references in the art, Petitioner asserts that an express motivation "for forming such an insulating layer over the metal source and drain electrodes" would be to provide "a good, level surface" for the OLED elements. *Id.* at 74 (Ex. 1018 ¶ 184). Relying on the testimony of Dr. Fontecchio, Petitioner further contends that such a modification "would have been an obvious design choice well known in the art and well within the knowledge and skill of a [person of ordinary skill in the art] at the time of the alleged invention of the '338 patent, as evidenced by [prior art references], each of which disclosed forming the OLED pixel electrode on top of a planar insulating layer," and further, that such an "obvious design choice[] would have actually simplified the

manufacturing process of Childs." *Id.* at 74–75 (citing Ex. 1018 ¶¶ 188–191).

In its Patent Owner Response, Patent Owner contends that Childs fails to satisfy this limitation under the agreed-upon district court construction for two reasons. PO Resp. 44 (citing Ex. 2005 ¶ 133). First, Patent Owner contends the pixel electrodes of Childs are not "on the surface" of the transistor array substrate because "large portions of the pixel electrodes are buried within and under the transistor array substrate." *Id.* (citing Ex. 2005 ¶ 133). Patent Owner also contends the pixel electrodes of Childs are not "arrayed along" or "located between" the interconnections because "parts of the pixel electrodes are almost directly beneath the interconnections." *Id.* at 45 (citing Ex. 2005 ¶ 133).

Patent Owner also responds to the proposed modification of Childs and asserts that neither "the references nor the Fontecchio declaration identify any benefit to adding this insulating layer to Child's existing design." *Id.* (citing Ex. 2005 ¶ 134). Patent Owner contends that Petitioner's proposed modification of adding a layer to Childs "will require further deposition and photolithography steps and will increase the cost of the device." *Id.* (citing Ex. 2005 ¶ 134). Patent Owner further contends that "the additional insulating layers are made from silicon nitride [which] would block the light [] emitted from the EL element." *Id.* Regarding the alternative modification of Childs to move the pixel electrodes "by placing them on top of layer 12," Patent Owner contends that modifying Childs in this manner would bring disadvantages such as reducing the brightness of the display that would prevent a person of ordinary skill in the art from making the modification. *Id.* at 46–47 (citing Ex. 2005 ¶ 137; Ex. 2007, 126:25–127:6). Patent Owner also contends that even if insulating layer 12

of Childs is replaced with a transparent insulator, "such as SiO_2 as Dr. Fontecchio suggests," unintended "light from EL elements will more easily hit transistors Tm" and will "cause unintended currents to flow through the transistors and may lead to failure of the device." *Id.* at 47 (citing Ex. 2005 ¶ 138; Ex. 2007, 74:21–75:4).

Regarding "arrayed along" and "located between," Petitioner asserts Patent Owner's "attempt to import this additional limitation [precluding parts of the pixel electrodes from being almost directly beneath the interconnections] is meritless." Pet. Reply 28 (citing PO Resp. 44–45). Petitioner contends the Specification of the '338 patent refutes such additional limitations and "describes a structure similar to Childs as the preferred embodiment (*see, e.g.*, Figure 6)." *Id.*

Regarding the requirement that the pixel electrodes be "on the surface" of the transistor array substrate, Petitioner explains that Childs discloses "the lower electrodes 21 are formed on insulating layer 8 in an exposed connection 'windows 12a' (i.e., trenches)" and Figure 2 depicts that "[w]here the pixel electrodes are located, insulating layer 8 is the top of the transistor array substrate." *Id.* at 29 (citing Ex. 1005, 8:16–27, Fig. 2); *see id.* at 29 n.6 (citing Ex. 1025, 103:20–104:17) (discussing how under the district court's construction of "transistor array substrate" as a "layered structure upon which or within which a transistor array is fabricated," insulating layer 8 could be considered the top of the transistor array substrate, thus, undoubtedly forming lower electrode 21 on the surface of the transistor array substrate).

In the alternative, Petitioner reiterates that it would have been obvious to a person of ordinary skill in the art "to modify Childs to form the lower electrode on the surface of its transistor array substrate." *Id.* (citing Pet. 71–

75; Ex. 1018 ¶ 179). Petitioner asserts that none of Patent Owner's alleged problems that may arise as a result of the modification to Childs are "substantiated, and each assumes a bottom-emitting device when . . . Childs explains its device may be used as a top[]-emitter." *Id.* at 30–31 (citing PO Resp. 46–47). Furthermore, Petitioner asserts that Patent Owner has not shown "that any of these alleged 'problems' would meaningfully impact the function of the device." *Id.* at 31. In particular, Petitioner contends "[Patent Owner] offers no evidence for its speculation that placing the lower electrode in a high level could 'lead to failure of the device' because it could increase the amount of light reaching transistors." *Id.* (citing PO Resp. 47). Petitioner asserts that Patent Owner's reliance upon Dr. Fontecchio's deposition is misplaced because "while Dr. Fontecchio agreed that using [a transparent] SiO_2 insulating layer may make it more likely that light reaches the transistors, [Dr. Fontecchio] did not agree that this would adversely affect the transistors' operation." *Id.* (citing PO Resp. 47; Ex. 2007, 74:21–75:4).

In its Sur-reply, Patent Owner asserts that Childs does not disclose, or render obvious, "a plurality of pixel electrodes . . . on the surface of the transistor array substrate." PO Sur-reply 21–25. Patent Owner reiterates that Child's lower electrodes are not "on the surface" of the transistor array substrate because "large portions of the pixel electrodes are buried ***under and in the alleged substrate***." *Id.* at 22 (citing Ex. 2005 ¶ 133). To illustrate this point, Patent Owner points to the specification of Childs that describes the embodiment as depicted in Figure 2 as having the "lower electrode 21 [] formed as a thin film ***in the circuit substrate 100***" and that the "window 12a [is] in a planar insulating layer 12 (for example of silicon

nitride) that ***extends over*** the thin-film structure of the substrate 100." *Id.* at 23; *see* Ex. 1005, 8:22–27.

Regarding the modification of Childs to form the lower electrode 21 on a different surface, Patent Owner reiterates its position that none of the references cited by Petitioner identify a benefit for adding further insulating layers and that doing so "will require further deposition and photolithography steps and will increase the cost of the device." PO Sur-reply 24 (citing Ex. 2005 ¶ 134). In particular, Patent Owner asserts that reliance on Kobayashi for adding insulating layers is insufficient because Kobayashi's insulating layers are formed from an opaque silicon nitride, which "would block light 250 emitted from the EL element." *Id.* Patent Owner also contends that Petitioner's reliance on references that teach the benefits of forming pixel electrodes on a flat surface is not applicable to Childs because "the surface of Childs that the pixel electrodes are deposited on is insulating layer 8, which is already flat in the areas where the pixel electrodes are deposited." *Id.* at 24–25 (citing Ex. 2005 ¶ 135).

Patent Owner reiterates the assertion that Child's lower electrodes are not "arrayed along" or "located between" the interconnections because "parts of the pixel electrodes are almost directly beneath the interconnections." *Id.* at 25. Patent Owner further contends that none of the proposed modifications to Childs would satisfy this limitation because none of the other references, including Kobayashi, would result in pixel electrodes that are "arrayed along" or "located between" the interconnections. *Id.* Patent Owner also asserts that Childs does not disclose the pixel electrodes being "arrayed along" the interconnections. *Id.* at 25–28. As discussed above, Patent Owner contends that "arrayed along [] must imply being adjacent to one another and some overlap in at least one of the

interconnections," and asserts "Childs simply does not meet this limitation." *Id.* at 25–26 (internal quotations omitted).

We find Petitioner has persuasively shown that Childs teaches this limitation. Childs states that the physical barriers 210 (including conductive barriers 240) are included "between at least some of the [neighboring] pixels in at least one direction of the array," and each neighboring pixel 200 includes a lower electrode 21. Ex. 1005, 7:10–12, 8:16–17, 8:23–9:1, Fig. 2. An exemplary pixel layout is shown in Figure 6 of Childs as reproduced below.

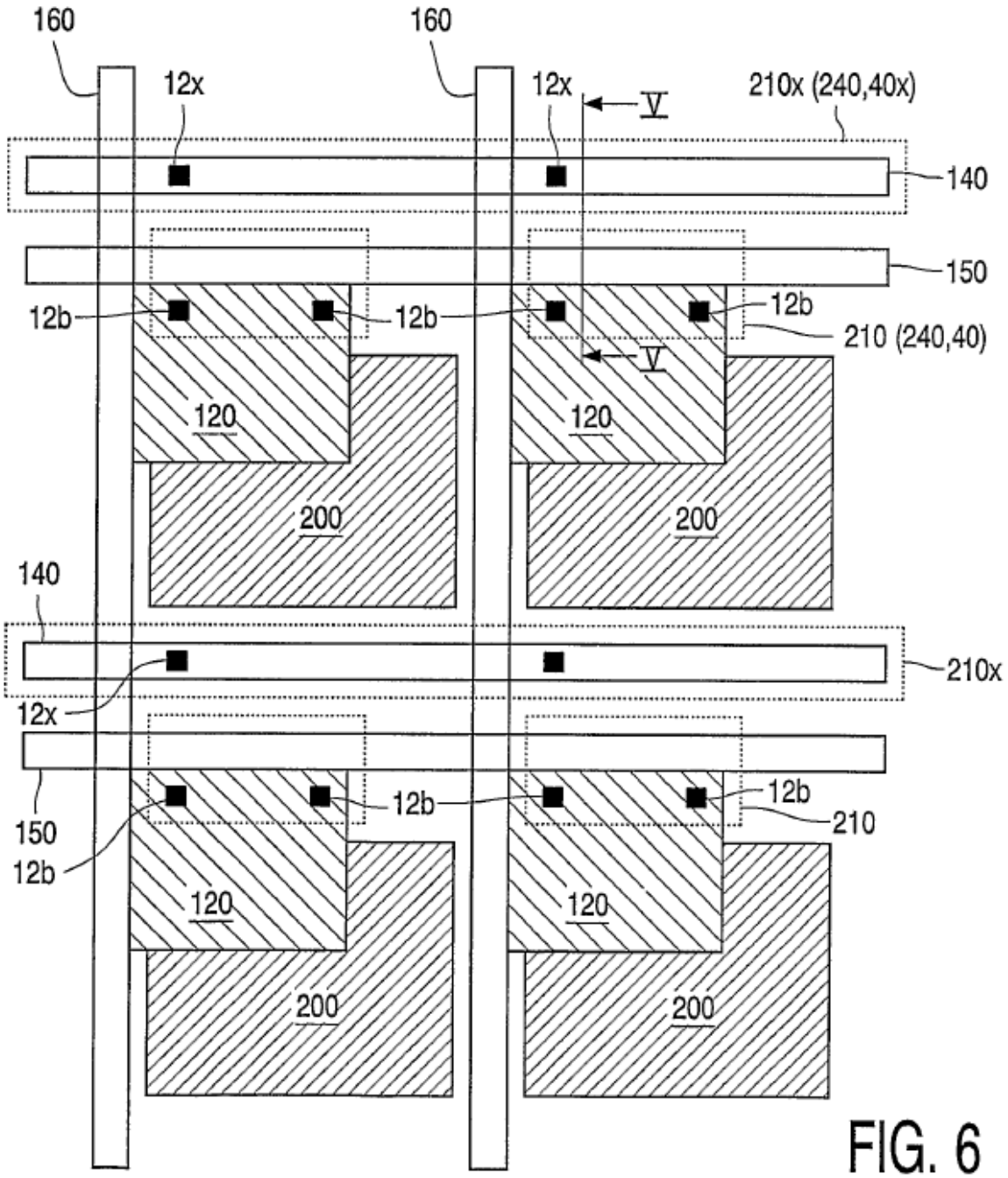


FIG. 6

Figure 6 of Childs shows a plan view of the physical barriers 210, 210x (including conductive barriers 240) arrayed between and extending along neighboring pixels 200 (including lower electrode 21, *see* Fig. 2 above). *Id.* at 11:10–21. This exemplary pixel layout shows conductive barriers 240, as part of physical barriers 210, are situated between and extend along lower

electrode 21, as included in pixels 200. Patent Owner's arguments to the contrary rely on claim constructions that we have not adopted as discussed above.

Regarding the pixel electrodes being arrayed on the surface of the transistor array substrate, we do not agree with Patent Owner that being arrayed on the surface requires the entirety of the pixel electrodes to be arrayed on the surface. PO Resp. 44 (citing Ex. 2005 ¶ 133); PO Sur-reply 22–23 (citing Ex. 2005 ¶ 133). As shown in the cross-sectional view of Figure 2 of Childs, lower electrodes 21 are disposed on the upper surface of the transistor array substrate at the trench, or window 12a, which appears as the top surface of the transistor array substrate at that portion, i.e., window. The fact that a portion of the lower electrodes 21 are within or under substrate 12 does not preclude the remaining portions from being disposed on the upper-most surface of the substrate at that area – window 12a. Patent Owner's arguments to the contrary rely on claim constructions that we have not adopted as discussed above. Accordingly, we determine Petitioner has shown Childs teaches the pixel electrodes being arrayed along the interconnections between the interconnections on the surface of the transistor array substrate.

Regarding the modification of Childs to form the lower electrode 21 on top of a different insulating layer instead of on exposed surface of insulating layer 8, we find Petitioner's contentions persuasive. Childs describes that "[a]part from constructing and using its barriers 210 with conductive material 240, the active-matrix electroluminescent display of a device in accordance with the present invention may be constructed using known device technologies and circuit technologies." Ex. 1005, 14:24–27. Childs describes that its "thin-film circuit substrate 100 with its upper planar

insulating layer 12 [and connection windows 12a are] manufactured in [a] known manner." *Id.* at 14:29–15:2. Thus, the known manufacturing steps in Childs include the lower electrode 21 and insulating layer 12 as depicted in Figure 14. *See id.* at 14:23–15:8.

We find persuasive Petitioner's contentions that it would have been obvious to form the lower electrode 21 on top of insulating layer 12 instead of exposing lower electrode 21 via windows 12a. Pet. 72–73 & n.7 (citing Ex. 1005, 8:24–27, 15:24–28, 16:21–24; Ex. 1018 ¶ 187); Pet. Reply 29–30 (citing Ex. 1018 ¶¶ 188–191). In particular, Childs discusses using both opaque silicon nitride and transparent silicon dioxide as materials used for insulating layers. Ex. 1005, 8:24–27, 15:24–28, 16:21–24. Although insulating layer 12 is described only with respect to silicon nitride, Childs appears to acknowledge the suitability of using either material as an insulating layer within the display device. *See id.* Thus, we are persuaded by Dr. Fontecchio's testimony that a person of ordinary skill in the art "would have recognized that forming the 'planar insulating layer 12' out of transparent silicon dioxide would allow light emitted by the OLED elements to pass through planar insulating layer 12 when the pixel anode electrodes 21 were formed on the surface of that planar insulating layer 12." Ex. 1018 ¶ 187.

We are also unpersuaded by Patent Owner's assertions that forming electrode 21 on a transparent insulating layer 12 would lead to device failure. In particular, the deposition testimony of Dr. Fontecchio and the declaration of Mr. Flasck, on which Patent Owner relies, establish only that additional light may reach transistors Tm. PO Resp. 47 (citing Ex. 2005 ¶ 138; Ex. 2007, 74:21–75:4). Light 250 must already pass through substrate 100 in the bottom-emitting configuration shown in Figure 2 of

Childs, and fabricating insulating layer 12 from a transparent material as opposed to an opaque material may allow additional emitted light to reach transistors, but the evidence before us does not support that this would lead to device failure as Patent Owner suggests. We also find persuasive Petitioner's contention that forming the lower electrode 21 on top of insulating layer 12 would have "merely [] required reordering the steps of Childs' fabrication process." Pet. 72–73 (citing Ex. 1018 ¶ 180). Although Petitioner does not rely upon the additional prior art references for this specific purpose, those references evidence the known nature of "forming the OLED pixel electrode on top of a planar insulating layer." *Id.* at 75; Ex. 1018 ¶¶ 181–185.

We also find that Petitioner has provided a persuasive rationale for making this modification to Childs, namely, to simplify the manufacturing process. In particular, reordering the manufacturing to first deposit aluminum electrodes 3 and 4, then deposit electrodes 21 after insulating layer 12 is "[a] common and straightforward way to prevent oxidation of the aluminum electrodes" by depositing "a protective insulating layer [12] over the aluminum [3 and 4] during formation of the indium tin oxide electrodes [21]." Ex. 1018 ¶¶ 188–191. Merely reordering the deposition fabrication, instead of adding an entirely new insulating layer, also avoids the additional manufacturing steps associated with protecting the aluminum electrodes and associated with etching the windows for the lower electrode. *See id.*

For the reasons discussed above, we find Petitioner has shown a person of ordinary skill in the art would have been motivated to reorder the manufacturing steps of Childs to first deposit a transparent insulating layer before depositing the lower electrode, thus placing the lower electrode on the surface of the transistor array substrate.

Claim 1 further recites "a plurality of light-emitting layers formed on the pixel electrodes, respectively." Ex. 1001, 24:26–27. Petitioner contends "Childs discloses that '[e]ach pixel 200 comprises a current-driven electroluminescent display element 25 (21, 22, 23),' and that 'a light-emitting organic semiconductor material 22' is formed 'between' each 'lower electrode 21 and an upper electrode 23.'" Pet. 75–76 (citing Ex. 1005, 7:10–12, 8:16–27, 9:3–11, 15:29–31; Ex. 1018 ¶¶ 194–195). We find these disclosures, cited by Petitioner, show that Childs discloses "a plurality of light-emitting layers formed on the pixel electrodes, respectively" as recited in claim 1. We note that Patent Owner does not separately address this limitation (*see generally* PO Resp.; PO Sur-reply).

Claim 1 also recites

> wherein said plurality of transistors for each pixel include a driving transistor, one of the source and the drain of which is connected to the pixel electrode, a switch transistor which makes a write current flow between the drain and the source of the driving transistor, and a holding transistor which holds a voltage between the gate and source of the driving transistor in a light emission period.

Ex. 1001, 24:31–38. Petitioner contends the combination of Childs and Shirasaki teaches this limitation. Pet. 76–82 (citing Ex. 1004 ¶¶ 3–8, 13–19, 41, 43, Fig. 5B; Ex. 1005, 1:5–7, 7:6–30, Fig. 1; Ex. 1018 ¶¶ 201–214). Specifically, Petitioner contends "Childs discloses that the plurality of transistors for each pixel include the claimed 'driving transistor' and 'switch transistor,' and it would have been obvious to further incorporate the claimed 'holding transistor' in view of Shirasaki." *Id.* at 76.

Again, Petitioner provides an annotated version of Figure 2 of the '338 patent and an annotated version of Figure 5B of Shirasaki (*id.* at 78–79), as Petitioner did for its challenge based on Kobayashi and Shirasaki. As

discussed above, those annotated figures show the three-transistor pixel circuits in the '338 patent and Shirasaki are substantially the same.

In explaining the combination of Childs' and Shirasaki's teachings, Petitioner argues a person of ordinary skill in the art would have replaced Childs' two-transistor pixel circuit with Shirasaki's three-transistor pixel circuit to "suppress[] the influence of variations in the voltage-current characteristic of the control system and allow[] the optical element to stably display images with desired luminance" and to "stably display image[s] with desired luminance in a display panel." *Id.* at 79–80 (citing Ex. 1004 ¶¶ 11, 18; Ex. 1018 ¶¶ 207–208). Petitioner supports replacing Childs' pixel circuit by pointing to Shirasaki's discussion of the disadvantages of two-transistor circuits. *Id.* at 79 (quoting Ex. 1004 ¶¶ 3–4, 7 ("difficult to display images with a desired luminance tone for long time periods"; "no accurate tone control"; "difficult to make the characteristics of the transistors [] of the individual pixels uniform"). Petitioner also notes Shirasaki teaches advantages of three-transistor pixel circuits over pixel circuits with four or more transistors, including lower power consumption and improved apparent brightness. *Id.* at 80 nn.9–10 (citing Pet. § VIII.A.1.1[f]; Ex. 1004 ¶¶ 9, 12, 19–20; Ex. 1018 ¶ 209).

Discussing the reasonable expectation of success, Petitioner contends that Shirasaki "expressly discloses that its three-transistor pixel circuit is meant to replace the two-transistor pixel circuit found in 'conventional light emitting element display' devices." *Id.* at 81 (citing Ex. 1004 ¶¶ 2–8, 13–19). Petitioner further contends that Childs and Shirasaki come from the same field of endeavor of "active matrix organic light-emitting diode display panels featuring thin-film transistor arrays." *Id.* (citing Ex. 1004 ¶¶ 41, 43; Ex. 1005, 1:5–7; Ex. 1018 ¶¶ 211–212). Petitioner also contends that a

person of ordinary skill in the art would have recognized Shirasaki's three-transistor circuit could have been implemented "without altering any of the layers above the transistor array substrate in Childs' layered OLED structure." *Id.* at 81–82 & n.11 (citing Ex. 1018 ¶¶ 213–215) (discussing implementing Shirasaki's three-transistor circuit would require "changing the photomasks used to fabricate the TFT array and relocating the 'windows' through Childs' 'planar insulating layer 12'" and that such steps "were routine and predictable manufacturing steps involved during the fabrication of every OLED display panel").

In its Patent Owner Response, Patent Owner asserts that a person of ordinary skill in the art would not have been motivated to replace Childs' two-transistor pixel circuit with Shirasaki's three-transistor pixel circuit. PO Resp. 35–43. Patent Owner raises similar arguments against this combination as it did against the Kobayashi-Shirasaki combination discussed above. *See id.*

In its Reply, Petitioner contends that Childs contemplates applying "its improvements to interconnections" to "alternative circuit structures [than] the two-transistor circuit structure provided in its example." Pet. Reply 22 (citing Ex. 1005, 7:5–9). Petitioner also reiterates the express teaching of Shirasaki to replace a two-transistor pixel circuit with Shirasaki's three-transistor pixel circuit to "suppress the influence of variations in the voltage current characteristic of the control system and allow[] the optical element to stably display images with desired luminance." *Id.* at 22–23 (citing Ex. 1004 ¶¶ 11, 18; Ex. 1018 ¶¶ 138–139).

Regarding reasonable expectation of success, Petitioner contends Childs leaves open the possibility of "other pixel configurations besides the two-transistor voltage-controlled system used." *Id.* at 24 (citing Ex. 1005,

7:6–9). Petitioner further contends that substituting Shirasaki's three-transistor circuit for Childs' two-transistor circuit "would have simply required changing the photomasks used to fabricate the TFT array and relocating the 'windows' through Childs' 'planar insulating layer 12' that connect[s] the TFT array to the OLED elements" and that such steps "were routine and predictable manufacturing steps in the fabrication of OLED display panels." *Id.* (citing Pet. 75; Ex. 1005, 14:29–15:2; Ex. 1018 ¶ 215).

Petitioner also addresses Patent Owner's argument that "the addition of a third transistor will reduce the light emitting area of each pixel and reduce the brightness and/or lifespan of the device." *Id.* at 25–27 (citing PO Resp. 42). First, Petitioner contends that Patent Owner's assertion is conclusory because Patent Owner "has not shown that adding a third transistor to Childs would actually increase the thin-film circuit area 120 shown in Figure 6" and Patent Owner's expert "repeat[s] the assertion near-verbatim with no factual explanation or citation to any evidence." *Id.* (citing PO Resp. 42–43; Ex. 2005 ¶¶ 128–129). Second, Petitioner contends that even if thin film circuit area 120 is increased, there is still room "in each pixel where a third transistor could be fabricated without impacting the light emitting area." *Id.* at 26–27 (citing Ex. 1005, Fig. 6). Third, Petitioner rebuts Patent Owner's arguments relying on a bottom-emitting device of Childs by noting Childs discloses a top-emitting (i.e., light 250 emitted through the top instead of the bottom substrate 100) configuration. *Id.* at 27 (citing Ex. 1005, 8:28–9:17).

We have considered the parties' arguments and evidence on this issue as detailed above, and we find Petitioner's contentions persuasive. As Petitioner asserts, "[Patent Owner] does not dispute that Shirasaki meets the circuit structure recited in [claim 1]." *Id.* at 4–5. Thus, the issue here

concerns the motivation to combine, namely, the motivation "to replace Childs's two-transistor voltage-driven pixel circuit with Shirasaki's three-transistor current-driven pixel circuit [as depicted in annotated Figure 5B of Shirasaki below]." Pet. 80; Pet. Reply 21; *see also* Tr. 27:10–19 (asserting Childs describes a conventional two-transistor circuit that Shirasaki teaches replacing). We agree with Petitioner that Shirasaki provides an express motivation for this change, namely, to "suppress the influence of variations in voltage-current characteristic of control system and allow[] the optical element to stably display images with desired luminance." Pet. Reply 22–23 (citing Ex. 1004 ¶¶ 11, 18; Ex. 1018 ¶¶ 138–139).

We disagree that a person of ordinary skill in the art would not have been motivated to modify Childs in view of Shirasaki because the two are allegedly directed to different problems. Instead, we agree with Petitioner that "Childs and Shirasaki are both directed to improving active matrix OLED panels featuring thin-film transistor arrays." *Id.* at 23; Pet. 79 (citing Ex. 1004 ¶¶ 41, 43; Ex. 1005, 1:5–7; Ex. 1018 ¶¶ 211–212).

Regarding the teachings of Shirasaki, we agree with Petitioner that Shirasaki discusses improving upon the background of conventional two-transistor circuits and teaches "replacing two-transistor voltage-controlled circuits, like the example in Childs, with its three-transistor current-controlled circuit." Pet. Reply 22–23 (citing Ex. 1004 ¶¶ 11, 18, Fig. 11; Ex. 1018 ¶¶ 138–139; Ex. 1025, 39:22–40:4). As discussed above regarding Petitioner's asserted combination of Kobayashi and Shirasaki, we consider whether one of ordinary skill would have been motivated to combine the teachings of both references as a whole, not whether the specific problems solved by the prior art are the same. Based on the record before us, we determine a person of ordinary skill in the art would have been motivated to

combine the teachings of Childs and Shirasaki as asserted by Petitioner, even if there are some particular differences in the specific problems addressed in those references.

Regarding reasonable expectation of success, we agree with Petitioner's explanation that the required manufacturing changes of "changing the photomasks used to fabricate the TFT array and relocating the 'windows' through Childs' 'planar insulating layer 12' that connect the TFT array to the OLED elements, [] were routine and predictable manufacturing steps." Pet. 81–82 & n.11 (citing Ex. 1018 ¶ 215; Ex. 1005, 14:29–15:2); Pet. Reply 24. As Dr. Fontecchio testifies, Childs describes a known manner of opening connections windows 12a–x in layer 12, i.e., pixel electrodes, by "photolithographic masking and etching." Ex. 1018 ¶ 215 (citing Ex. 1005, 14:29–15:2).

Regarding Patent Owner's assertions the Petitioner fails to account for the unmodified "write current" of Childs, we find, for the same reasons as discussed with respect to Patent Owner's arguments on Kobayashi's unmodified "write current" above, that replacing the two-transistor circuit of Childs with the three-transistor circuit of Shirasaki entails incorporating the write current (memory current) of Shirasaki's circuit. Pet. Reply 12–13 (citing Pet. 55; PO Resp. 25–26). In particular, Petitioner notes that "the 'memory current' α that flows in Shirasaki's three-transistor circuit when 'transistor 11' (the claimed 'switch transistor') 'is turned on,' . . . is the same as 'pull-out current' A shown in annotated Fig. 2 of the '338 patent." *Id.* at 13–14 (citing Pet. Supp. Br. 3 (citing Ex. 1004 ¶¶ 72, 84, Fig. 5a; Ex. 1001, 15:34–37, Fig. 2)). Thus, we determine Petitioner has sufficiently shown a reasonable expectation of success for its proposed modification.

For the reasons discussed above, we determine Petitioner has shown a person of ordinary skill in the art would have been motivated to replace Childs' two-transistor circuit with Shirasaki's three-transistor circuit to include a switch transistor that makes a write current flow between the drain and the source of the driving transistor. In sum, for the reasons discussed above, we determine Petitioner has shown by a preponderance of the evidence that claim 1 is unpatentable as obvious over Childs and Shirasaki.

Dependent claims 2, 3, and 5–13

Petitioner provides further analysis detailing where it contends each additional limitation of claims 2, 3, and 5–13 are taught in Childs, which we find sufficiently persuasive. Pet. 82–92.

Claim 2 depends from independent claim 1 and additionally recites:

> wherein said plurality of interconnections include at least one of a feed interconnection connected to the other of the source and the drain of at least one of the driving transistors, a select interconnection which selects at least one of the switch transistors, and a common interconnection connected to the counter electrode.

Ex. 1001, 24:39–44. Petitioner contends a person of ordinary skill in the art "would have understood this claim to require that the plurality of interconnections include at least one of the three types of claimed interconnections . . . as opposed to requiring all three types of claimed interconnections, as recited by dependent claim 4." Pet. 83 (citing Ex. 1018 ¶ 216). Petitioner further contends that Childs teaches feed interconnections "connected to the other of the source and the drain of at least one of the driving transistors." *Id.* (citing Ex. 1018 ¶ 216). We are persuaded because Childs states its "conductive barrier 240" can be "connected to and/or from one or more circuit element," with one of those circuit elements being the

"supply line 140," which is connected to drive TFT T1. Ex. 1005, 7:10–17, 9:20–29, Fig. 1; Ex. 1018 ¶ 217. Petitioner also contends that Childs teaches select interconnections "which select at least one of the switch transistors." Pet. 84. For example, Childs discloses its "conductive barrier 240" can supplement and/or replace "addressing line 150," which transmits "selection signal that turn on the addressing TFT T2." *Id.* (citing Ex. 1005, 7:18–22, 9:20–29, Fig. 1; Ex. 1018 ¶ 218) (internal quotations omitted). We note that Patent Owner does not separately address this claim (*see generally* PO Resp.; PO Sur-reply).

Claim 3 further depends from claim 2 and additionally recites "wherein each of the light-emitting layers is formed between two of the feed interconnection, the select interconnection, and the common interconnection." Ex. 1001, 24:44–47. Petitioner contends Childs discloses the light-emitting pixels 200 are formed between the projecting interconnections 210 and 210x. Pet. 85 (citing Ex. 1005, 11:11–21, Figs. 5–6; Ex. 1018 ¶¶ 220–221). We find this contention persuasive. For example, Childs states: "Figure 5 illustrates a composite of two side-by-side barriers 210 and 210x, each comprising a metal core 240, 240x," and Figure 5 depicts pixels 200 (as a light emitting layer) formed between 210 and 210x. Ex. 1005, 11:11–21, Figs. 5–6. We note that Patent Owner does not separately address this claim (*see generally* PO Resp.; PO Sur-reply).

Claim 5 depends from independent claim 1 and additionally recites "wherein said plurality of pixels include a red pixel, a green pixel, and a blue pixel." Ex. 1001, 24:53–54. Petitioner contends Childs teaches its plurality of pixels "include red pixels, green pixels, and blue pixels." Pet. 86–87. We are persuaded because Childs states its barriers "prevent pixel overflow of conjugate polymer materials that may be ink-jet printed for red, green and

blue pixels of a color display." Ex. 1005, 1:20–2:1. Petitioner contends, and we are persuaded, that a person of ordinary skill in the art would have recognized such disclosure "was directed for use in a conventional color OLED display, which [was] well known to require and include red, green, and blue pixels." Pet. 86–87 (citing Ex. 1018 ¶ 223 (citing Ex. 1007)). We note that Patent Owner does not separately address this claim (*see generally* PO Resp.; PO Sur-reply).

Claim 6 further depends from claim 5 and additionally recites "wherein said plurality of pixels comprises a plurality of sets each including the red pixel, green pixel, and blue pixel arrayed in an arbitrary order." Ex. 1001, 24:55–58. Petitioner contends Childs teaches this limitation. Pet. 87 (citing Ex. 1005, 1:20–2:1; Ex. 1018 ¶ 225). We are persuaded because Childs states its barriers "prevent pixel overflow of conjugate polymer materials that may be ink-jet printed for red, green and blue pixels of a color display." Ex. 1005, 1:20–2:1. Petitioner contends, and we are persuaded, a person of ordinary skill in the art "would have recognized that [Childs'] red, green, and blue pixels would be arrayed into sets of three pixels each including a red, green, and blue pixel in an arbitrary order, as disclosed by numerous contemporary prior art references that discussed color OLED displays." Pet. 87 (citing Ex. 1018 ¶ 225). We note that Patent Owner does not separately address this claim (*see generally* PO Resp.; PO Sur-reply).

Claim 7 depends from independent claim 1 and additionally recites "wherein at least one of the interconnections has a thickness of 1.31 to 6.00 μm." Ex. 1001, 24:59–60. Petitioner contends Childs discloses this limitation. Pet. 87 (citing Ex. 1005, 10:30–11:2; Ex. 1018 ¶ 227). We are persuaded because Childs states: "the conductive barrier material 240 may have a thickness Z" and "[i]n a specific example Z may be between 2 μm

and 5 μm." Ex. 1005, 10:30–11:2. We note that Patent Owner does not separately address this claim (*see generally* PO Resp.; PO Sur-reply).

Claim 8 depends from any one of claims 1 or 2–7, and additionally recites "wherein at least one of the interconnections has a width of 7.45 to 44.00 μm." Ex. 1001, 24:61–63. Petitioner contends Childs discloses this limitation. Pet. 88 (citing Ex. 1005, 11:3–6; Ex. 1018 ¶ 228). We are persuaded because Childs states: "the conductive barrier material 240 may have a line width Y" and "[i]n a specific example Y may be 20 μm." Ex. 1005, 11:3–6. We note that Patent Owner does not separately address this claim (*see generally* PO Resp.; PO Sur-reply).

Claim 9 depends from independent claim 1 and additionally recites "wherein at least one of the interconnections has a resistivity of 2.1 to 9.6 μΩcm." Ex. 1001, 24:64–65. Petitioner relies upon the testimony of Dr. Fontecchio that "the resistivity of the interconnections depends on the material used to construct them." Pet. 88 (citing Ex. 1018 ¶ 229 (citing Ex. 1003)). Petitioner also relies upon the disclosure of the '338 patent that "when an Al-based material or Cu is used," a certain range of resistivity of 2.1 to 9.6 μΩcm results. *Id.* (citing Ex. 1005, 10:6–10, 16:27–28; Ex. 1001, 21:58–62; Ex. 1018 ¶ 229). Petitioner contends that Childs meets this limitation, and we are persuaded, because Childs states "pixel barriers 210 . . . are predominantly of electrically-conductive materials 240, 240x, preferably metal for very low resistivity (for example aluminum or copper or nickel or silver)." Ex. 1005, 10:6–10, 16:27–28. We note that Patent Owner does not separately address this claim (*see generally* PO Resp.; PO Sur-reply).

Claim 10 depends from independent claim 1 and additionally recites "wherein said plurality of interconnections are formed from a conductive

layer that is different from a layer forming the source and the drain of each of the transistors and a layer forming the gate of the transistors." Ex. 1001, 24:66–25:3. Petitioner contends Childs discloses its "conductive metal barriers 240" are formed from a different conductive layer than the source, drain, and layer forming the gate of the transistors. Pet. 88–89 (citing Ex. 1005, 8:3–15, 10:6–10, Fig. 2; Ex. 1018 ¶ 231–232). For example, Childs discloses "electrically conductive material 240, 240x, [is] preferably metal for very low resistivity (for example aluminium or copper or nickel or silver)" and "an active semiconductor layer 1 [of transistors] (typically of polysilicon); a [transistor] gate dielectric layer 2 (typically of silicon dioxide); a gate electrode 5 (typically of aluminium)." Ex. 1005, 8:3–15, 10:6–10. We find Petitioner's contentions are supported by the cited disclosures. We note that Patent Owner does not separately address this claim (*see generally* PO Resp.; PO Sur-reply).

Claim 11 depends from independent claim 1 and additionally recites "wherein said plurality of interconnections are formed from a conductive layer different from a layer forming the pixel electrodes." Ex. 1001, 25:4–6. Petitioner contends Childs discloses its "conductive metal barriers 240" are formed from a different conductive layer than the lower electrodes. Pet. 90 (citing Ex. 1005, 8:19–22, 10:6–8; Ex. 1018 ¶¶ 234–235). For example, Childs discloses "electrically conductive material 240, 240x, [is] preferably metal for very low resistivity (for example aluminium or copper or nickel or silver)" and "lower electrode 21 may be an anode of indium tin oxide (ITO)." Ex. 1005, 8:19–22, 10:6–8. We find Petitioner's contentions are supported by the cited disclosures. We note that Patent Owner does not separately address this claim (*see generally* PO Resp.; PO Sur-reply).

Claim 12 depends from independent claim 1 and additionally recites "wherein said plurality of interconnections are thicker than a layer forming the source and the drain of each of the transistors and a layer forming the gate of each of the transistors." Ex. 1001, 25:7–10. Petitioner contends in Childs, the conductive barrier material 240 has a thickness Z that is a factor more than the source and drain of the transistors along with the layer forming the gate of each transistor. Pet. 91 (citing Ex. 1005, 10:30–11:1, Fig. 2; Ex. 1018 ¶¶ 237–238). For example, Childs discloses: "electrically conductive material 240 may have a thickness Z that is a factor of two or more (for example at least five times) larger than the thickness z of this conductor layer 5 (150) in the circuit substrate 100," and the conductor layer 5 forms the gate. Ex. 1005, 10:30–11:1. Petitioner then relies upon Figure 2 of Childs to depict how conductive metal barriers 240 are "substantially thicker than both layer 1 that forms the source and drain of each of the transistors, as well as layer 5 that forms the gate of each of the transistors." Pet. 91 (citing Ex. 1018 ¶¶ 237–238). We find Petitioner's contentions are supported by the cited disclosures. We note that Patent Owner does not separately address this claim (*see generally* PO Resp.; PO Sur-reply).

Claim 13 depends from independent claim 1 and additionally recites "wherein said plurality of interconnections are thicker than the pixel electrodes." Ex. 1001, 25:11–12. Petitioner contends Childs discloses the conductive barrier material 240 as thicker than lower electrode 21. Pet. 92 (citing Ex. 1005, 8:22–24, 10:30–11:1; Ex. 1018 ¶¶ 239–240). For example, Childs discloses "conductive barrier material 240 may have a thickness Z that is a factor of two or more (for example at least five times) larger than the thickness z of this conductor layer 5 (150) in the circuit substrate 100" and the "the lower electrode 21 is formed as a thin film in the circuit

substrate 100." Ex. 1005, 8:22–24, 10:30–11:1. Petitioner also relies upon Figure 2 of Childs to illustrate "how the conductive metal barriers 240 . . . are substantially thicker than layer 21 that forms the pixel electrodes." Pet. 92 (citing Ex. 1018 ¶¶ 239–240). We find Petitioner's contentions are supported by the cited disclosures. We note that Patent Owner does not separately address this claim (*see generally* PO Resp.; PO Sur-reply).

For the reasons discussed above, we determine Petitioner has demonstrated by a preponderance of the evidence that claims 1–3 and 5–13 would have been obvious over Childs and Shirasaki.

IV. CONCLUSION[12]

For the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–3 and 5–13 of the '338 patent are unpatentable, as summarized in the following table.

[12] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this Decision, we draw Patent Owner's attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

Claims	35 U.S.C. §	Reference(s) /Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
1, 2, 5, 6, 9–11	103(a)	Kobayashi, Shirasaki	1, 2, 5, 6, 9–11	
1–3, 5–13	103(a)	Childs, Shirasaki	1–3, 5–13	
Overall Outcome			1–3, 5–13	

V. ORDER

Accordingly, it is:

ORDERED that claims 1–3 and 5–13 of the '338 patent are held to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to this proceeding seeking judicial review of our decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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